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A Calibration Service for Analog-to-Digital and Digital-to-Analog Converters

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CONTENTS

	Page
Abstract	1
1. INTRODUCTION	1
1.1 Intended Applications	2
1.2 Parameters Measured	2
1.3 General Test Strategy	3
2. SPECIFICATIONS FOR TEST CONVERTERS	4
2.1 Preparation of Test Boards	4
3. TEST CAPABILITIES	4
4. NBS DATA CONVERTER TEST SET	6
4.1 Approach	7
4.2 ADC RMS Noise Measurement	9
4.3 Design Features	13
4.3.1 Reference DAC	13
4.3.2 Error Measurement and Digitizing Circuitry	14
4.3.3 Auto-Offset and -Gain Circuitry	14
4.3.4 Transition-Locking Feedback Loop	16
4.3.5 Noise Measurement Circuit	16
4.3.6 Universal Code Converter	19
4.3.7 Operation and Control	19
4.3.8 Isolation and Grounding	20
5. CHECK STANDARDS	22
5.1 18-bit DAC	22
5.2 18-bit ADC	22
6. TEST PROGRAMS AND PROCEDURE	25
6.1 Basic Linearity Test	25
6.1.1 Walsh Function Analysis	27
6.1.2 Analysis of Less Significant Bits	33
6.2 Random Code Test	33
6.3 Differential Linearity Test	34
6.4 ADC Noise Test	36
7. TEST SET CALIBRATION AND QUALITY CONTROL	39
7.1 Reference DAC	39
7.2 Offset and Gain Errors	39
7.3 Accuracy of Error Measurement Circuitry	40
7.4 ADC Noise Measurement	40
7.5 Overall System Performance	41
8. ERROR ANALYSIS	41
8.1 Linearity Error	41
8.1.1 DAC-20	41
8.1.2 Error Measuring Circuitry	44
8.1.3 ADC Feedback Loop Errors	44
8.1.4 Total Estimated Uncertainty	44
8.2 Bit Coefficients	45
8.3 Differential Linearity Errors	46
8.4 Offset Error	46
8.5 Gain Error	46
8.6 ADC RMS Input Noise	47

CONTENTS (cont.)

	Page
9. CALIBRATION REPORTS	47
10. ACKNOWLEDGMENTS	61
11. REFERENCES	61
APPENDIX A. Test Board Preparation and Documentation	62

LIST OF FIGURES

	Page
Figure 1. Data converter test set: simplified diagram	8
Figure 2. Noise measurement technique based on response of transition-locking feedback loop	10
Figure 3. Noise response of feedback loop: converter input voltage versus clock periods	12
Figure 4. Graph of relationship between the noise ratio $\sigma/\Delta V$ and the slope reversal probability P	12
Figure 5. System clock and counter circuits for error digitizing ,	15
Figure 6. Auto-offset and gain circuitry . . ,	15
Figure 7. Transition-locking feedback loop	17
Figure 8, Noise measurement technique showing digital circuitry to estimate probability of slope reversals	18
Figure 9, Isolation and grounding	21
Figure 10. Simulation ADC and its connection to test set	23
Figure 11. Periodicity of first three Rademacher functions	28
Figure 12(a). Linearity error data for converter having low superposition errors (14-bit DAC)	31
Figure 12(b). Linearity error data for converter having relatively large superposition errors (16-bit ADC)	32
Figure 13. Typical results of random code test: linearity error (1 LSB/DIV) versus output code (minus full scale to plus full scale)	35
Figure 14, Hypotheses test for ADC noise measurement	38
Figure 15. Typical linearity error data for NBS 18-bit DAC check standard	42
Figure 16. Typical linearity error data for NBS 18-bit ADC check standard (simulation ADC)	43

LIST OF FIGURES (cont.)

	Page
DAC Report Figure 1. Linearity error data	52
ADC Report Figure 1. Linearity error data	57
ADC Report Figure 2. Equivalent rms input noise: measured noise versus output code	58
Figure A-1. Suggested printed circuit board for test data converter	66

A CALIBRATION SERVICE FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS

T. M. Souders, D. R. Flach,
and B. A. Bell

An NBS calibration service for high performance 12- to 18-bit analog-to-digital converters (ADC's) and digital-to-analog converters (DAC's) is described. The service offers comprehensive measurements of linearity, differential linearity, gain, offset, and rms input noise (for ADC's), with systematic uncertainties as low as 3 ppm. Measurements are made at a minimum of 1024 different code-words. The measurement approach, design features, test programs and data reduction techniques are documented, as are the methods of error estimation and quality control. Representative reports of tests are included for both DAC's and ADC's.

Key words: analog-to-digital converter; calibration service; data converter; differential linearity; digital-to-analog converter; error measurement; gain; input noise; linearity; offset.

1. INTRODUCTION

Analog-to-digital converters (ADC's) and digital-to-analog converters (DAC's) are devices fundamental to almost all modern measurement and control instrumentation. Over the past decade, both converter applications and capabilities have undergone dramatic expansion. With this growth, increased attention is being focused on appropriate measurement support. The extensions in resolution alone from the 10- to 12-bit capabilities of several years ago to the 16 to 18 bits achievable today imply not only a 64-fold increase in performance, but also represent a comparable increase in the number of discrete states available and a corresponding increase in the number of calibration points potentially required,

To address these needs, a calibration service based on an automated test facility has been developed at the National Bureau of Standards for measuring the static transfer characteristics of high-performance ADC's and DAC's. This service specifically addresses the measurement of static converter errors, i.e., the deviation of the actual from the ideal response when the input is held at a fixed value. A capability for making dynamic measurements is currently under development.

1.1 Intended Applications

The calibration service is particularly intended for the following customer applications:

1. Testing of high resolution converters for use in unique, highly demanding applications.
2. Satisfying traceability requirements imposed by State, Federal or military contracts.
3. Independently verifying the test methods of converter manufacturers through the use of transfer standards.
4. Verifying incoming inspection tests of converter users by the same use of transfer standards.
5. Periodically testing high resolution converters used in precision automatic test equipment.
6. Providing performance data during development stages of new converter products.

While the test methods and standards employed in this calibration service can, in principle, be duplicated in customers' laboratories, it may rarely be cost-effective, since only a relatively few converters demand the same high levels of accuracy.

1.2 Parameters Measured

The principal error parameters measured are those of linearity and differential linearity [1]¹. Nevertheless, gain and offset errors may also be measured when appropriate, and the equivalent rms input noise of ADC's can be measured as well. Determination of monotonicity in DAC's and missing codes in ADC's is not generally performed since it requires excessive measurement time for high resolution converters. These characteristics can often be inferred, however, from the linearity data available. Sensitivity of these various parameters to changes in temperature and power supply voltage, for example, is also not generally determined.

Since no standards for data converter terminology exist, the definitions of these parameters follow:

1. Linearity Error: The difference between the actual and ideal levels of the static input/output characteristic after offset and gain errors have been removed.

¹Numbers in brackets refer to the literature references listed at the end of this report.

2. Differential Linearity Error: The difference between the actual and ideal separation between adjacent levels.
3. Offset Error: The difference between the actual and ideal levels, measured at the negative-most level of the input/output characteristic. (Due to practical considerations discussed later, this definition is modified to the 2nd most negative level, i.e., with the least significant bit (LSB) on.)
4. Gain Error: The difference between the actual and ideal levels, measured at the positive-most level of the input/output characteristic, after the offset error has been removed. (Again, in practice, a defining level is chosen slightly below the one stated here.)
5. Equivalent RMS Input Noise- The rms value of the effective internal noise of an ADC, referred to its input terminals.

In each of these definitions, the specified levels are taken to be: for DAC's, the discrete output levels, and for ADC's, the analog input levels at which the digital output transitions between adjacent codes occur. In this latter case, the transition levels are defined by the upper digital code of the transition in question.

1.3 General Test Strategy

Since many high accuracy, high speed ADC's, and almost all DAC's operate with intrinsically fixed values assigned to each individual binary digit, any output or input codeword (comprised of a serial combination of these bits) has an assigned value theoretically equal to the sum of the values of the individual bits that are included. Were it not for small interactions between the bits and other code dependent effects collectively called superposition errors, n measurements would suffice to completely characterize the 2^n code states of an n -bit converter. Because significant superposition errors frequently do exist, the NBS test facility is equipped to measure many, if not all, of the 2^n states.

Typically, all 1024 digital codeword combinations of the 10 most significant bits are measured. Errors contributed by the remaining less significant bits are generally insignificant, a premise which is tested during the calibration process. From the test data are calculated the offset and gain errors, and the linearity errors associated with each tested codeword.

While most converter manufacturers traditionally specify the linearity errors of their products by a single figure representing the maximum error occurring over the entire transfer characteristic, a great deal of information is, of course, hidden by the single figure of merit. If, for example, a single code of a 14-bit ADC exhibits an error having

twice the magnitude of any remaining codeword errors, the converter may be rejected on the basis of a single code error which occurs, on the average, only once in over 16 000 conversions. Taking another example, if the value of bit 2 of a high resolution DAC has drifted out of specified tolerance since its adjustment at the factory, a simple screwdriver adjustment of a built-in trimmer might be all that is required to bring the converter back within specified tolerance again. On the other hand, if significant superposition effects are the primary cause of linearity errors, reduction through any simple means is generally impossible. For high resolution converters, such conditions are not uncommon. Therefore, it is the intent of this calibration service to provide data adequate for customers to recognize the source and distribution of errors, so that the information can be applied as best suits their individual needs. Accordingly, the data is analyzed for maximum, minimum and rms errors and is further processed to determine the effective errors of the individual bits, as well as the superposition errors.

2. SPECIFICATIONS FOR TEST CONVERTERS

To be compatible with the NBS data converter test set, test units must conform to the specifications given in table 1.

2.1 Preparation of Test Boards

In general, it will be the customer's responsibility to mount integrated circuit, hybrid, or modular test converters on suitable test boards, providing all required trimmer circuits, voltage references, input or output amplifiers, recommended power supply decoupling capacitors, and connectors for interfacing to the input/output lines. Fully self-contained converters need only be fitted with the necessary interfacing connectors. In so doing, the customer gains significant performance advantages while at the same time saving the additional fee which would otherwise be charged by NBS for performing this service. High performance converters are often susceptible to small changes in grounding, routing of dynamic signal lines, capacitive loading, etc. Particularly with ADC's, signal dynamics is quite important, even for static testing, since the converter itself always operates at high speeds. When mounted by the customer, the test converter and its support circuitry can be laid out more closely to the way in which it will be used in practice, as well as to the specific recommendations of its manufacturer. The test results should therefore more closely describe the converter's in situ performance. Detailed type and wiring requirements for the interfacing connectors are given in appendix A.

3. TEST CAPABILITIES

The systematic uncertainties in measuring the various converter error parameters are analyzed in section 8, and their estimated limits are summarized in table 2. Random errors of the measurement process necessarily include random variations in the test converter and are

therefore individually evaluated for each test (section 6.2). Nevertheless, measurements on very **stable** (check standard) converters indicate the random errors contributed by the test set itself are less than the respective systematic uncertainties listed in the **table**.

All values are **expressed** relative to full-scale range, or in the case of ADC input noise, the measured rms value.

Table 1

Parameter	Specifications of Test Converters	
	DAC's	ADC's
Resolution (Bits)	12-18	12-16
Voltage Ranges (V)	0-10; ± 10 ; 0-5; ± 5	
Output Load Capability	10 k Ω 100pF	-----
Input Impedance	-----	$\geq 200 \Omega/V$
Coding	Full Parallel Input or Output: Binary Unipolar Offset Binary Two's Complement One's Complement Sign-Magnitude Binary Complemented Versions of Above	
Acceptable Convert Command	20 μ s positive pulse for DAC's with input latches	2 μ s positive pulse
Status Output Command	-----	Required
Logic Compatibility	TTL	
Settling Time	<2ms	-----
Conversion Time	-----	$\leq 100 \mu$ s
External Power Requirements	$\pm 15V$, +5V	
Maximum error including gain & offset	500 ppm	

Table 2

Parameter	Estimated Systematic Uncertainty	
	DAC's	ADC's
Linearity Error: ± 10 V range 0-10 V, ± 5 V 0-5 V	2.7 ppm + 0.04 LSB	4.7 ppm + 0.16 LSB
	3.5 ppm + 0.04 LSB	5.5 ppm + 0.16 LSB
	4.2 ppm + 0.04 LSB	6.2 ppm + 0.16 LSB
Bit Coefficients	0th	same as linearity error same as for linearity error, less 0.06 LSB
	1st to 10th	same as linearity same as for 0th coef., less 1 ppm
Differential Linearity Error: ± 10 V 0-10 V, + 5 V 0-5 V	3.2 ppm + 0.04 LSB	5.2 ppm + 0.16 LSB
	4.2 ppm + 0.04 LSB	6.2 ppm + 0.16 LSB
	5.2 ppm + 0.04 LSB	7.2 ppm + 0.16 LSB
Offset Error ^a	3 ppm	3 ppm + 0.07 LSB
Gain Error ^a	6 ppm	6 ppm + 0.13 LSB
RMS Input Noise	-----	-100%; +(20% + 10 μ V) Noise introduced by Test Set is 30nV/ $\sqrt{\text{Hz}}$ in a 1 MHz BW.

^a Measured upon special request only, and only if no adjustable trimmers are provided for these parameters.

4. NBS DATA CONVERTER TEST SET

A number of measurement and design criteria for this test set have been established.

1. Since significant superposition errors are not uncommon in high resolution converters [2], a large number of, if not all, digital code states must be measured, requiring relatively fast automatic testing.
2. A resolution of 20 bits (1ppm) is needed for characterizing converters of 16 or 18 bits.
3. Gain, offset, linearity, and differential linearity errors must be measured, as well as the equivalent rms input noise of ADC's.

4. The measurements must be made in the presence of significant converter noise.
5. Flexibility is required in terms of accommodating various **binary coding formats and voltage ranges.**
6. The test set **is** to be operable in a manual as **well** as automatic mode, permitting fast troubleshootings, special tests, etc., without first writing and entering computer code. Finally, it is desirable for the ADC and DAC test circuits to share **common** test circuitry as far as is practicable.

A number of data converter test methods of varying complexity, resolution, and versatility have been described in the literature 13-51. None have been **specifically** addressed, however, to the **comprehensive** testing of higher resolution (>12 bits) converters,

4.1 Approach

Basic operation of the test set involves a comparison of the test unit with a DAC standard (see fig. 1). The standard presently in use is a multirange 20-bit plus sign, relay-switched converter previously developed at NBS [6]. It exhibits less than 1 μm linearity error and incorporates a self-calibration feature.

For testing DAC's, the standard and unit-under-test are both driven with the same digital input code and their respective analog outputs are compared. The difference in outputs is **amplified**, averaged over a 60-Hz period, and digitized. The data are displayed on the front panel and returned to the controller for logging and analysis. An auto-offset and gain (AOG) function is provided in which the data corresponding to the negative and **positive** full-scale endpoints of the **input/output** characteristic are latched, scaled, and fed back to the error measuring circuitry. This forces the endpoints of the transfer characteristic to coincide for the standard and unit-under-test. With the AOG circuit in use and updated periodically, error data are then a direct measure of linearity errors, independent of gain and offset drift, which **may** be monitored separately. **Any** of the 2^n codewords can be measured in this way.

Characterizing ADC's is more complex. Each digital output code corresponds to a continuous range of analog input values, the extremes of which are defined in terms of the corresponding digital transitions. A complete determination of the analog-to-digital transfer **characteristic** requires the location and measurement of each of these **transition** levels.

Transition **level** location is accomplished automatically by placing the converter under test within a feedback loop controlling the input voltage [5]. The upper digital code of the transition under

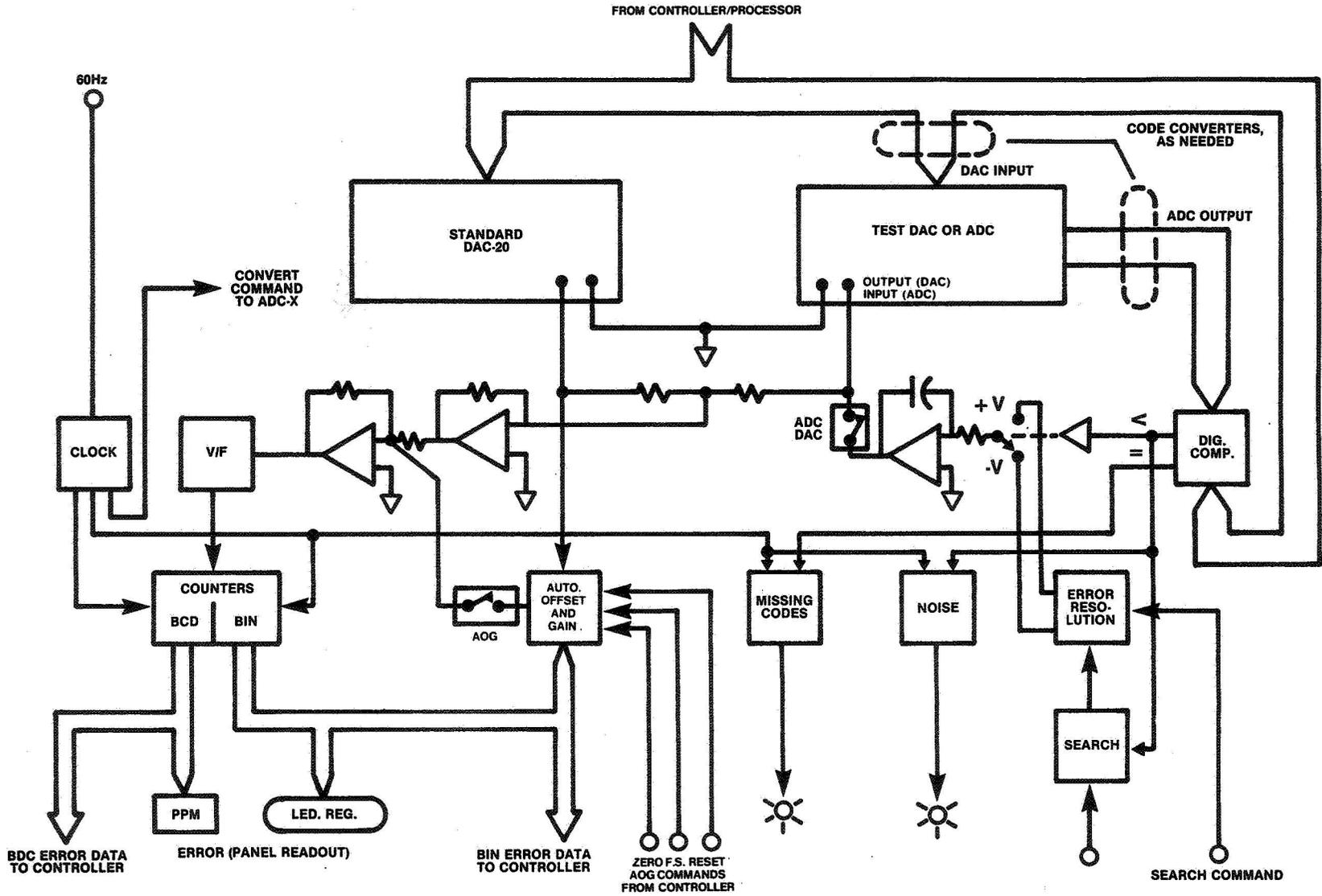


Figure 1. Data converter test set: simplified diagram

'investigation is presented to a digital comparator whose other input monitors the converter's digital output.

The digital comparator's less than output sets the polarity of a programmable input voltage (from the block marked error resolution) to an operational integrator, whose output in turn supplies the input voltage to the ADC under test. This voltage will ramp up (or down) until the transition in question is detected, whereupon the slope of the integrator's output voltage reverses. The process continues at a preset clock rate (normally 10 kHz) maintaining the ADC input very near the transition level. The precision with which the feedback loop locks onto the transition is determined by the overshoot, which in turn is a function of integrator input voltage, integration time constant, and analog-to-digital conversion rate. The integrator input voltage is programmable, and is typically set to give a precision of 1/16 LSB.

Having been located, the transition voltages are then measured by comparison with the reference voltage provided by the DAC standard, set to the same digital code. The comparison is performed with the same circuitry described above for DAC testing.

Additional logic circuits detect missing codes, initiate a fast search routine to speed the location of transitions, and implement an algorithm which provides an estimate of the equivalent rms input noise in the ADC under test.

The transition-locking feedback loop employed in this test set offers several advantages over other measurement approaches employing a DAC to directly excite the ADC under test. First, the transition is automatically located with high precision in the presence of significant noise in the test unit itself. Second, a wide-band very-low-noise output amplifier operating with essentially unity noise gain can be selected as the integrating amplifier which excites the ADC input. Furthermore, since the feedback loop locks onto the transition voltage of the test converter, drifts due to time or temperature in the feedback amplifier itself are not as critical as they would be in a reference DAC's output amplifier. Third, the feedback loop can be used to implement an algorithm facilitating an automatic Measurement of the equivalent rms input noise of the ADC, as described next.

4.2 ADC RMS Noise Measurement

In this technique [7], the noise measurements are made in the vicinity of the converter's decision levels represented by code transitions, where the noise sensitivity is greatest. These transition levels are located and locked onto with the feedback loop controlling the input voltage to the converter under test as previously described (see fig. 2). The actual rms noise measurement is based on a theoretical relationship between input noise and an expected number of counts derived digitally from the response of the feedback circuit.

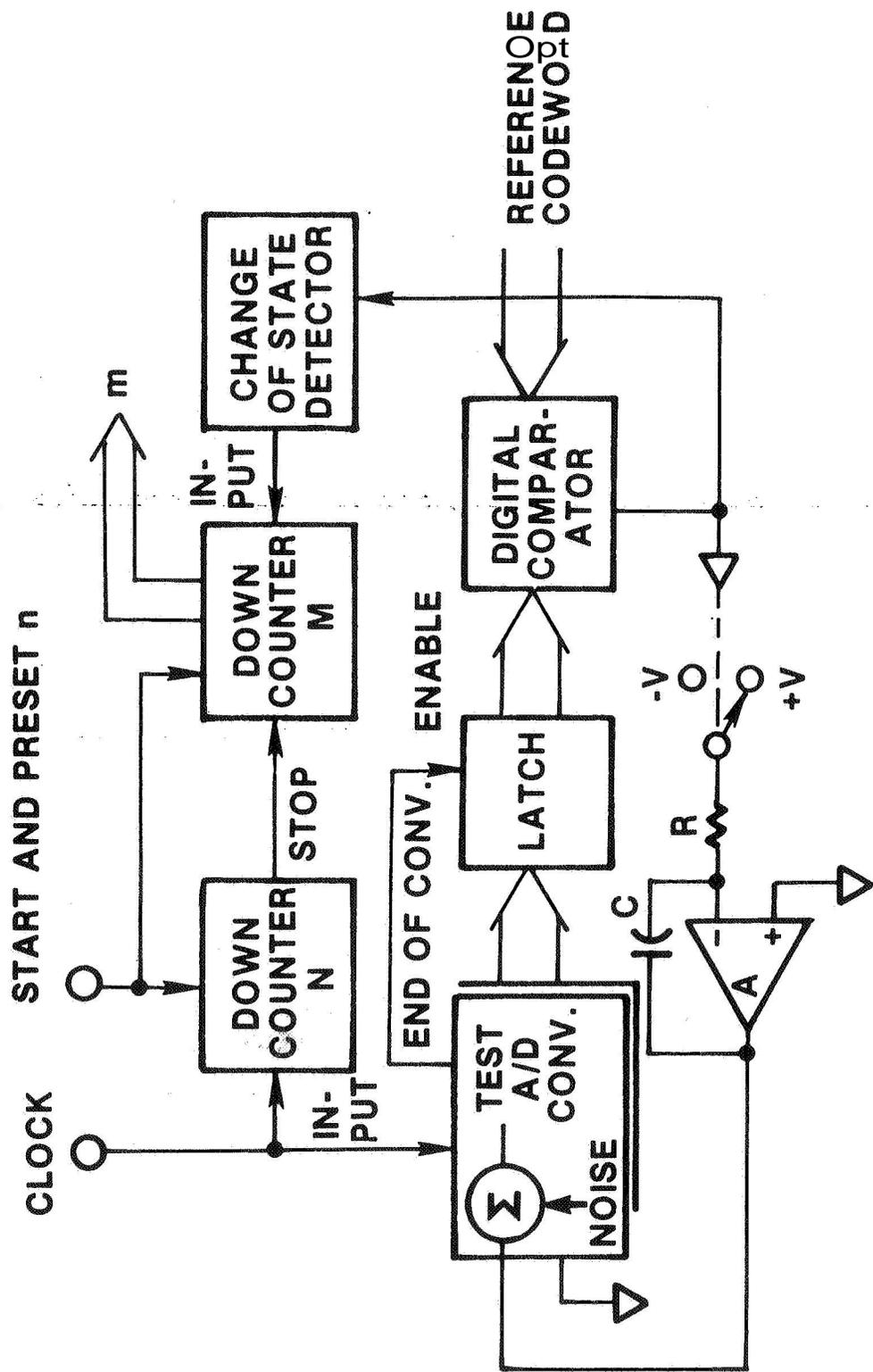


Figure 2. Noise measurement technique based on response of transition-locking feedback loop

With a noiseless ADC in the feedback loop, the input voltage change, once locking has occurred, will reverse its slope after each conversion describing a triangular waveform with ΔV peak-to-peak amplitude, as in figure 3-a. (The magnitude ΔV is determined by clock period, integration time constant, and integrator input voltage. Its value is set from the front panel.) The addition of random noise of rms value a at the ADC input causes a corresponding change in the feedback response, as shown in figure 3, b-d. The input voltage now follows a "random walk" about the transition level, reversing its slope with decreasing frequency (and straying farther from the transition level) as the noise level increases. If, at the given sampling rate, the successive values of noise are uncorrelated and follow a Gaussian distribution, the statistics of the random walk can be calculated in terms of the rms noise level. An easily measured statistical parameter has been selected which can form the basis for an equivalent noise measurement made in terms of the voltage ΔV . In particular, the probability P of occurrence of a slope reversal following a conversion is easily measured with digital circuitry, and can be accurately related to noise level as described in reference [7]. Since ΔV provides the reference voltage for the measurement of noise value a , it is convenient to express P in terms of the ratio $\sigma/\Delta V$.

A plot of the ratio $\sigma/\Delta V$ vs the calculated reversal probability P is given in figure 4. Over the $\sigma/\Delta V$ range of 0.4 to 8.0, this curve is described by the following expression

$$\sigma/\Delta V = \frac{A+BP}{1-2P}, \text{ where } A = -0.70 \text{ and } B = 0.60 \quad (1)$$

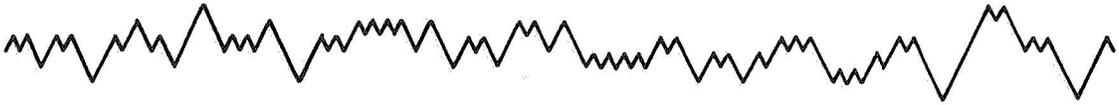
with an uncertainty of 1 percent in $\sigma/\Delta V$. These results assume that:

1. The magnitude ΔV is constant for positive and negative rates of change,
2. Noise from the integrating amplifier is negligible, and
3. The noise has a Gaussian distribution, and at the given sampling rate, successive values are uncorrelated.

The digital circuitry responsible for the measurement of probability P , and thus the rms noise a , is discussed in the following section.

A mathematical analysis of this technique is provided in reference [7], together with a discussion of error sources and experimental verification.

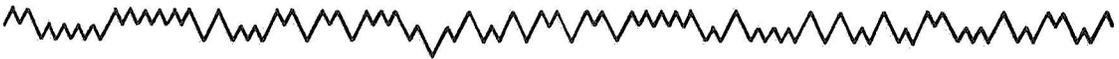
(d) RMS Noise = $2 \Delta V$ P = 0.59



(c) RMS Noise = $1 \Delta V$ P = 0.66



(b) RMS Noise = $0.5 \Delta V$ P = 0.75



(a) RMS Noise = $0 \Delta V$ P = 1.00



Figure 3. Noise response of feedback loop: converter input voltage versus clock periods

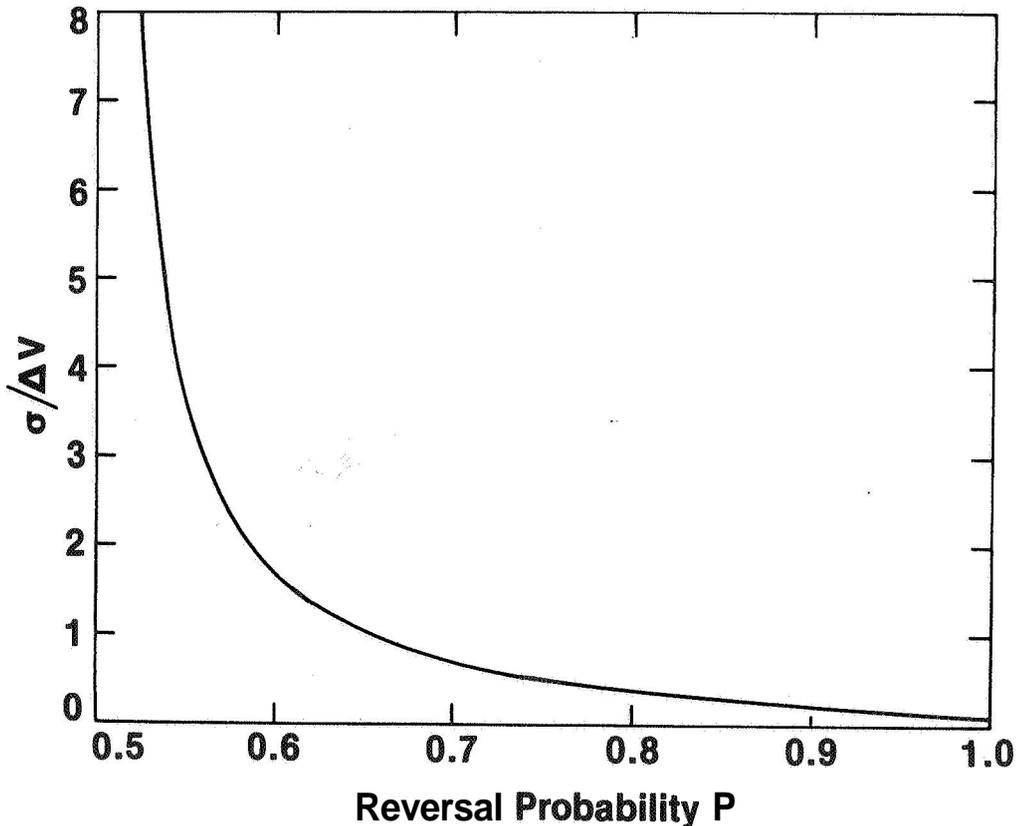


Figure 4. Graph of relationship between the noise ratio $\sigma/\Delta V$ and the slope reversal probability P

4.3 Design Features

Significant design considerations and operating features of the various subassemblies of the test facility follow.

4.3.1 Reference DAC

The 20-bit DAC serving as a reference standard for the test set is based on an R-2R ladder network used in the current switching mode. This configuration has the advantages of having only two binarily related resistor values, **low-voltage** current switching, constant power dissipation in the resistors regardless of switch positions, as well as easy implementation of a self-calibration technique. The **1 ppm limit** of linearity error of this instrument results from several different features.

1. A highly stable reference is provided by 10 electronically buffered, unsaturated standard cells in series, enclosed in a temperature controlled air bath.
2. Stable, hermetically sealed bulk-metal resistors having tracking temperature coefficients of less than $\pm 0.5 \text{ ppm}/^\circ\text{C}$ are used in all critical positions.
3. Latching, mercury-wetted relays are used for current switching, exhibiting approximately $1 \text{ m}\Omega$ contact repeatability. Thermal emfs are held to acceptable levels by using very short (-2.5 ms) switching pulses to the drive coils, thereby reducing the average power input.
4. Critical operational amplifiers have been selected to have open-loop gain in excess of 120 dB, very low offset drift with time and temperature, low offset and bias currents, and low noise.
5. A simple, easily operated self-calibration feature has been included which permits the linearity of the eight most significant bits to be measured and adjusted if necessary.

The following table gives the pertinent specifications:

- Code Format - Binary Sign-Magnitude
- Voltage Ranges - $\pm 10\text{V}$, $\pm 5\text{V}$, $\pm 2.5\text{V}$
- Resolution - 20 bits + sign, i.e., $10\mu\text{V}$, $5\mu\text{V}$ and $2.5\mu\text{V}$, respectively, on the 10V , 5V and 2.5V ranges, bipolar and unipolar
- Conversion Rate - $100/\text{s}$, max.
- Linearity Error - less than 1 ppm of Full-Scale Range ($\pm 10\text{V}$) after self-calibration

- Temperature Coefficients (gain, offset, linearity) - less than 0.5 ppm/°C each, near room temperature. The laboratory in which it is used is controlled to within ±0.5°C.

Further details are given in reference [6].

4.3.2 Error Measurement and Digitizing Circuitry

Error detection and amplification is accomplished in three stages with high gain, low offset and drift amplifiers. The first, most critical stage is a summing amplifier which takes the arithmetic sum of the output of the reference DAC and the input (output) of the ADC (DAC) under test. The summing resistors are 10 kΩ, have low, matched temperature coefficients, and show negligible load coefficients. Gain is selectable to provide direct reading errors for either unipolar or bipolar converters, and to accommodate special tests. The intermediate stage also receives signals from the auto offset and gain circuit and an offsetting current to implement offset binary coding in the following analog-to-digital conversion.

The amplified, offset, and gain corrected error signal is digitized with an integrating analog-to-digital conversion system comprised of a 100-kHz V/F converter and gated counters. By using two sets of counters, binary and BCD coded, and slightly different gating times for each as shown in figure 5, the error data is simultaneously digitized and appropriately scaled for direct reading in bits or digits with 20 bit and 1 ppm resolution, respectively. The BCD output, displayed in a decimal panel readout, provides direct readout of error in parts per million. The maximum error without overflow is in the 11th bit or 2⁻¹¹. By gating the counters over a 60-Hz period, determined by a clock phase-locked to the power line, 60-Hz and higher frequency noise is filtered. (The BCD counters are gated over a 10³/2¹⁰ fraction of a 60-Hz period for direct reading.)

4.3.3 Auto-Offset and -Gain Circuitry

The AOG function is accomplished by first strobing the minus full-scale (offset) error data into a latch. The latched data is fed to the IC multiplying DAC in the top half of figure 6, causing a corresponding offsetting current to be injected into the error measuring circuitry. A second error measurement, now offset corrected, at plus full scale is then taken. This new data is strobed into the second multiplying DAC. There the full-scale error data is multiplied by the output voltage of the standard DAC, and thus supplies a linearly code-dependent gain correction to the error measuring circuitry. Both offset and gain errors are thus automatically corrected.

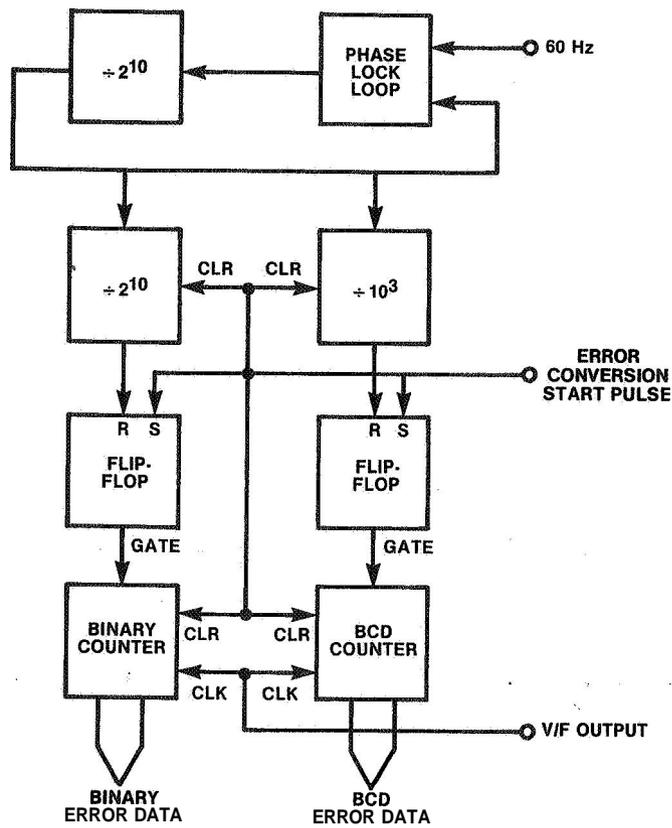


Figure 5. System clock and counter circuits for error digitizing

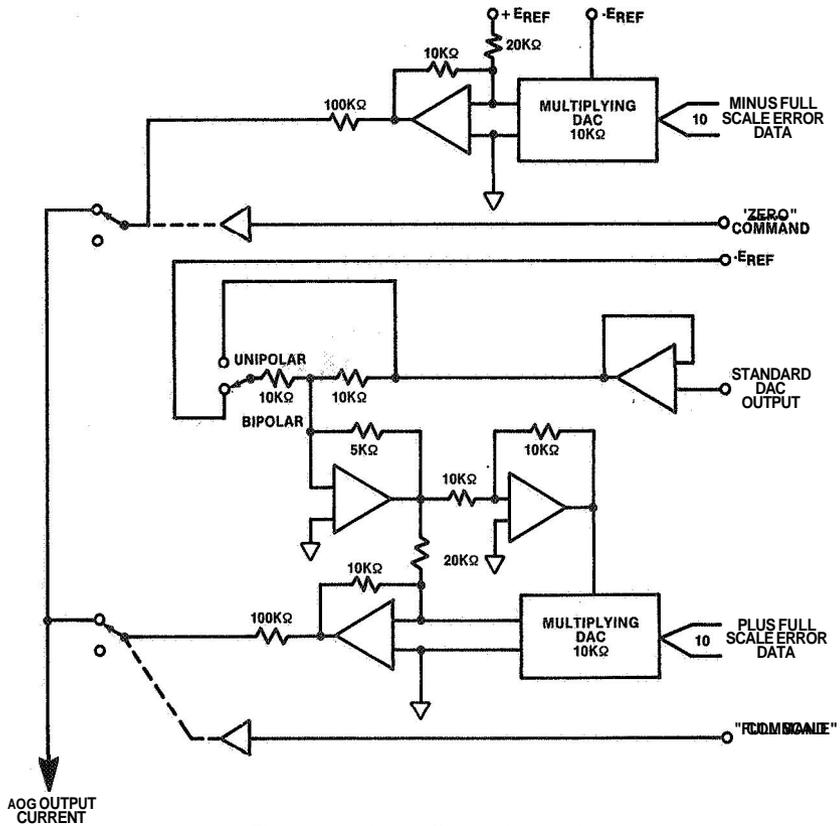


Figure 6. Auto-offset and gain circuitry

4.3.4 Transition-Locking Feedback Loop

Figure 7 presents the transition-locking circuitry in somewhat more detail. The integrator output voltage change per clock period is given by

$$\Delta V = \frac{V_r}{2^n} \cdot \frac{\Delta t}{RC} \quad (2)$$

where V_r is the reference voltage; 2^n is the attenuating factor determined by the multiplying DAC, Δt is the clock period, and RC is the integrator time constant. The proportional change is then

$$\frac{\Delta V}{V_r} = \frac{1}{2^n} \cdot \frac{10^{-4}}{10^{-1}} \approx \frac{1}{2^{(n+10)}} \quad (3)$$

for $t = 10^{-4}$ s and $RC = 10^{-1}$ s. The exponent n is selected from the front panel to provide the desired resolution (normally 1/16 LSB), adjustable from $1/(2^{(10+10)}) \approx 1$ ppm to $1/(2^{(0+10)}) \approx 0.1$ percent. To facilitate a rapid search for a far removed code transition, the exponent n can be set to zero, either from a front panel search button or by computer control, until the transition is reached, whereupon n is automatically returned to its preset value.

Important design considerations for this circuit include minimizing amplifier offsets and bias currents to maintain equal magnitudes of voltage changes (ΔV) per clock period for both positive and negative slopes. A match to 1 percent is adequate to assure a consistent definition of the transition voltage, the point at which 50 percent of the resulting output codes are above and 50 percent are below the transition. The accuracy of the noise algorithm will be assured as well. It is also important to minimize the average value of switching transients introduced in the circuit through the analog switch. While the transients themselves occur after an analog-to-digital conversion has been completed and thus do not affect the test unit directly, they nevertheless contribute to the average value of the transition voltage measured by the error-measuring circuitry. Finally, since ADC's with unbuffered inputs impose an active load having high frequency components during the conversion period, it is important to choose a wideband, low dynamic output impedance amplifier for the operational integrator.

4.3.5 Noise Measurement Circuit

The measurement of slope reversal probability can be accomplished with the digital circuitry functionally depicted in figure 8. The start

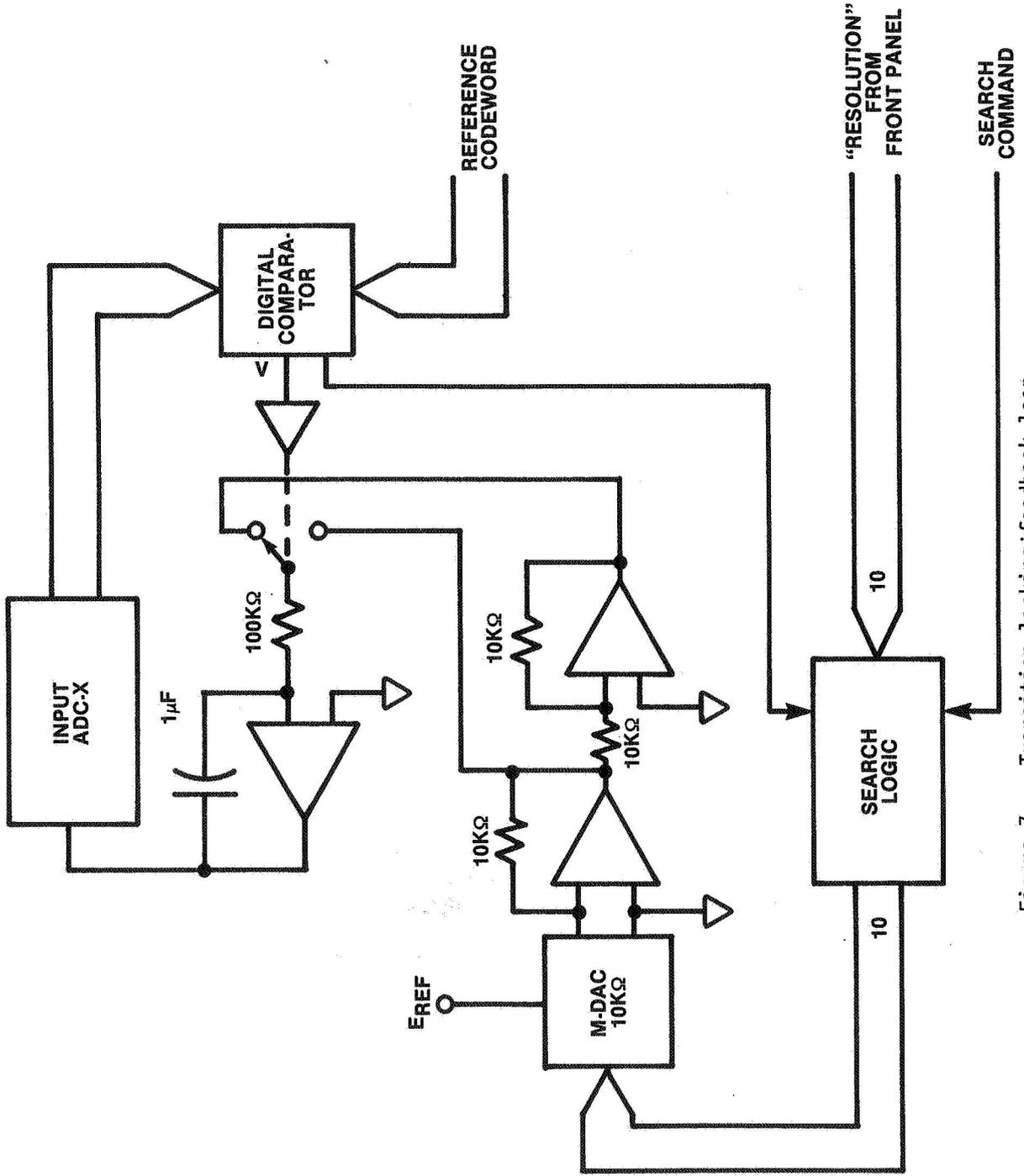


Figure 7. Transition-locking feedback loop

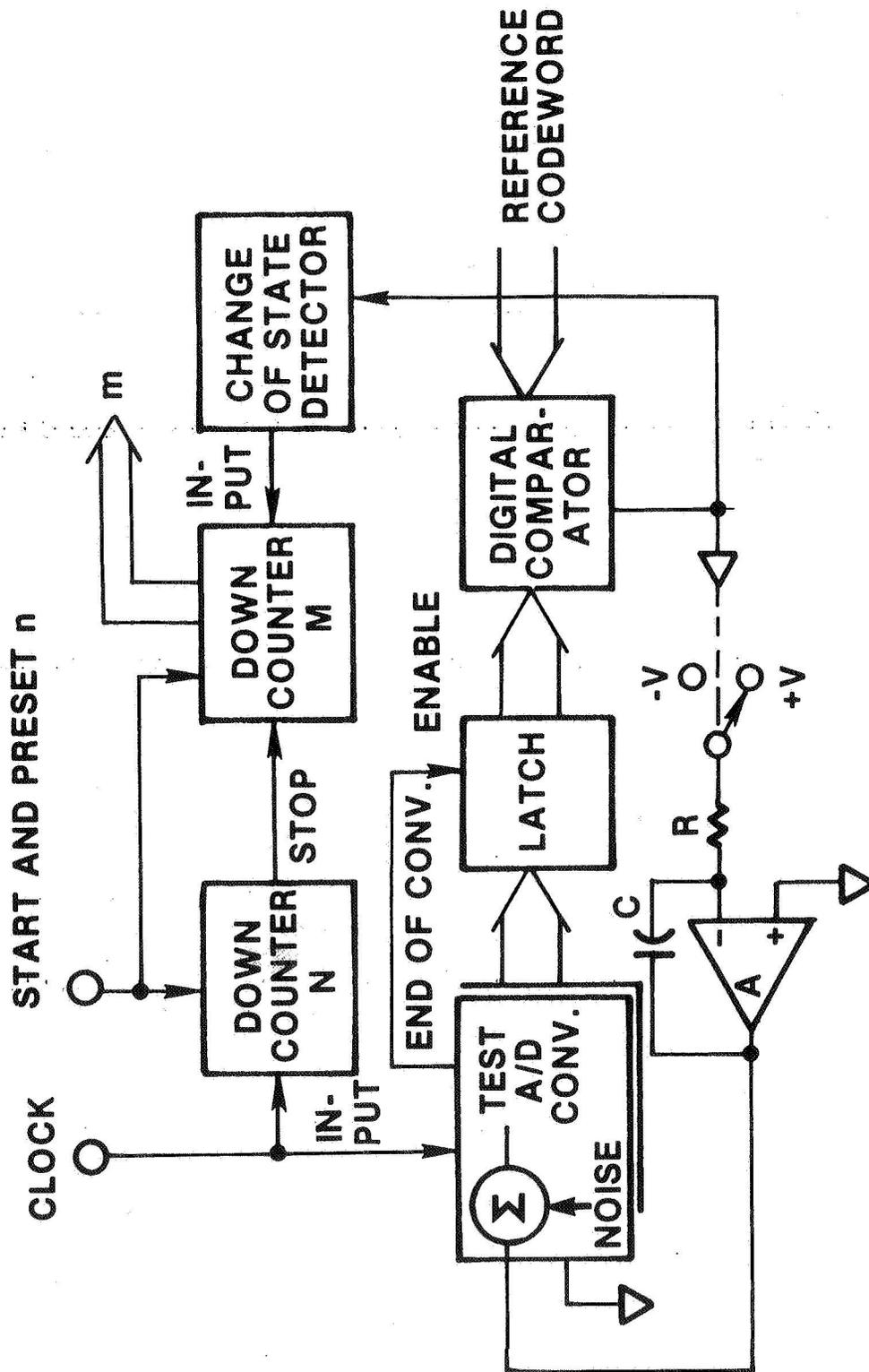


Figure 8. Noise measurement technique showing digital circuitry to estimate probability of slope reversals

command presets each down counter with the value n , and initiates counting. Changes in state of the digital comparator output (controlling the input voltage slope) decrement counter M via the change of state detector until n clock periods have been registered by counter N, stopping the test. The final value m held in counter M, subtracted from and divided by n , is an estimate of the reversal probability. Thus, for example, for $n = 100$, $n-m$ is the reversal probability in percent. For the test set described here, the stop pulse from counter N is actually the same pulse which gates the binary counters of figure 5, and therefore has a duration of 16.67 ms, or 166 (10 kHz) clock cycles. Consequently, noise data is available and returned to the controller concurrently with linearity error data, after each codeword measurement. To facilitate a simple pass-fail indication for the test panel, counter M is preset to 110 before each measurement. Since 110 is 66 percent of 166, this reference value corresponds to the probability value (0.66) for which $\sigma/\Delta V = 1$ (see fig. 4). Therefore, an underflow condition on counter M is an indication that $a < AV$, representing an acceptable noise level with respect to the threshold level AV set from the front panel. Because the relative standard deviation of a noise measurement can be rather large for a sample size of 166 clock periods [7], the noise data from a number of successive measurements is generally averaged. The process will be given in more detail in a later section (6.4).

4.3.6 Universal Code Converter

The 20-bit DAC standard uses sign-magnitude coding. When testing DAC's with other code formats, an appropriate code conversion is performed on the incoming sign-magnitude words before routing them to the test unit. For ADC testing, the test unit output codewords, when other than sign-magnitude, are converted to sign-magnitude coding before routing them to the digital comparator circuit. Both of these code converter functions are performed by a universal hardwired 20-bit code converter board, whose input and output codes may be independently selected among sign-magnitude, 1's complement, 2's complement, and off-set binary.

4.3.7 Operation and Control

The test panel contains controls to set up the operating conditions specific to each converter under test, including:

1. Device selection (ADC or DAC),
2. Polarity (bipolar or unipolar),
3. Range,
4. Code format,
5. Resolution of test, AV (for ADC's).

These parameters are not under control by the computer. The six operating functions may be initiated from front panel pushbuttons as well as from the controller. These are

1. Reset (reset AOG latches),
2. Offset (load minus full-scale error data),
3. Gain (load full-scale error data),
4. Load (load test word to standard and test units),
5. Search (search for distant code transitions),
6. Error (measure error and automatically display on panel).

Test codewords may be entered manually from a toggle register or automatically via the controller. With these functions, individual test points are easily set up and executed manually as well as under program control. The digital data output from the test set is in parallel binary format for both linearity and noise data, with provision for handling interrupts from missing code, noise, and overflow circuits. Digital input codewords are accepted in parallel binary format.

Automatic control is provided by an intelligent graphic display terminal via the IEEE 488 bus. Interface to the test set is made through an optically isolated 488 bus-to-parallel binary coupler. All computer code is written in BASIC.

4.3.8 Isolation and Grounding

To avoid serious errors which readily arise from ground loops, care has been taken to achieve essentially single point grounding. Accomplishing this condition required the use of several independent power supplies as well as both optical and relay isolation of signals. The general isolation and grounding system employed is illustrated in figure 9. Six independent power supplies are shown, together with coded blocks indicating the test system circuitry served by each. Interconnecting analog and digital signal lines (terminating with arrows), optical and relay isolation, and power supply grounding connections are also shown. Not shown are analog signal common connections for the test set and unit-under-test which are made at the ground tie point, indicated in the figure. The power supply ground line that remains common to both analog and digital signals is in the test set itself. In addition to the analog signals from the reference DAC and unit-under-test, it carries only micro-ampere-level signals required by the CMS multiplying DAC's in the AOG and error resolution circuits, and the CMS switch controlling the input voltage to the operational integrator. Of these signals, only the last one is dynamic during the actual measurement period, and it changes state only after the ADC-under-test has completed a conversion.

As mentioned above, the signal common connection for the test converter is made separately to the common ground tie point of the test set.

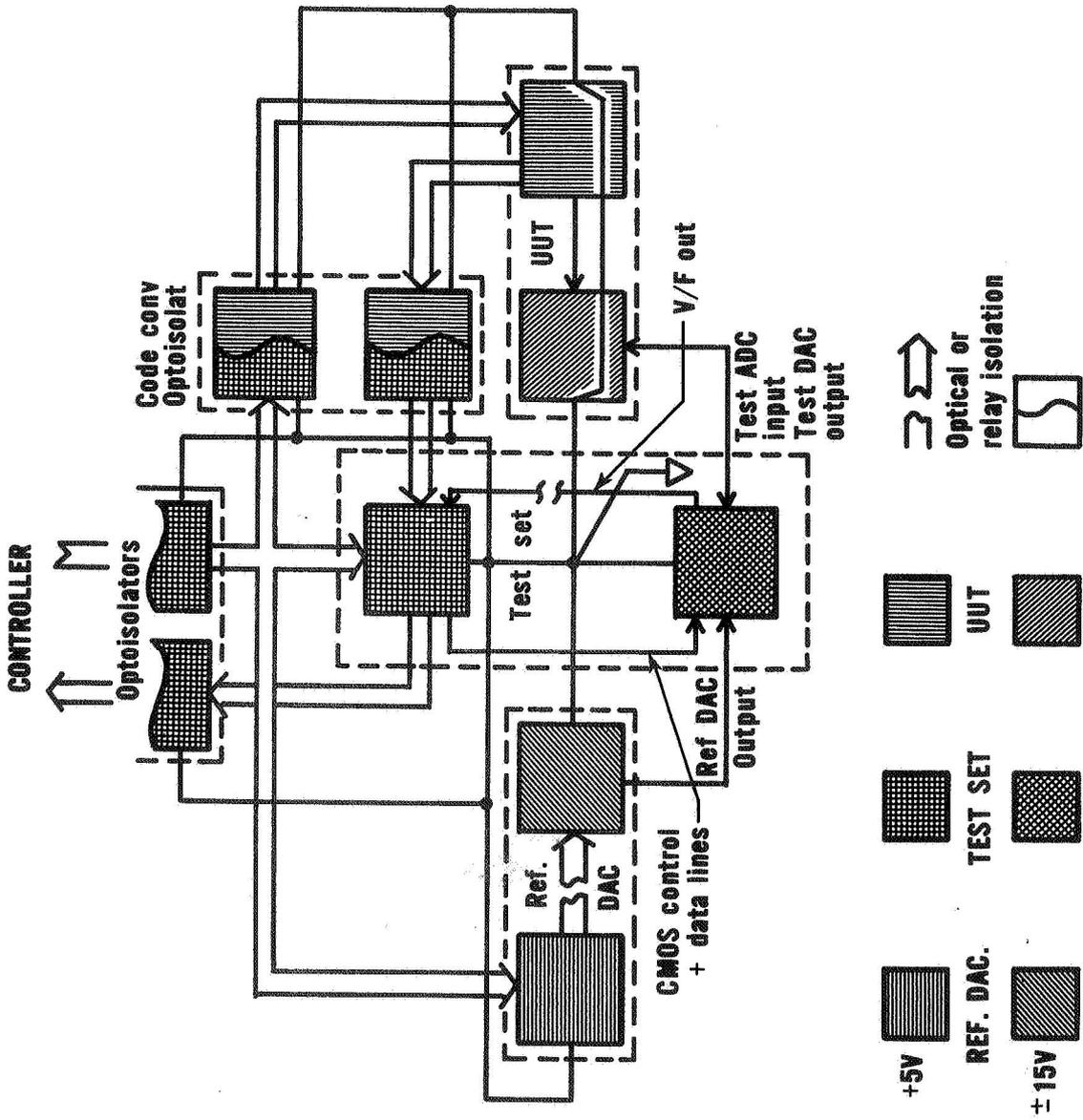


Figure 9. Isolation and grounding

5. CHECK STANDARDS

5.1 18-bit DAC

For purposes of performance verification and quality control, test units which have been independently developed and characterized are particularly well suited, provided they are of sufficient accuracy and stability. While commercially available data converters cannot yet reliably meet and maintain the <2 ppm limit of linearity error required for such service, a high-speed, low-noise 18-bit DAC developed at NBS is well suited for this purpose [8]. While optimized for low noise and fast settling, DAC-18 exhibits excellent static behavior as well. A temperature regulated voltage source based on standard cells provides a highly stable reference voltage, and the use of precision wirewound resistors and chopper stabilized amplifiers for the individual current sources ensures accurate, stable bit coefficients. The load resistors across which the output voltage is developed are also of precision wirewound construction and have very small load coefficients. The overall DAC has been temperature compensated. The measured offset, gain, and linearity temperature coefficients are less than 0.5 ppm, 0.3 ppm, and 0.4 ppm per $^{\circ}\text{C}$, respectively. The temperature variation of the laboratory in which the calibration service is conducted is ± 0.5 $^{\circ}\text{C}$. Linearity adjustment of DAC-18 is made independently, with a calibration procedure relying only on a reference source having short-term stability, and a precision Kelvin-Varley divider. Individual bits are adjusted as usual to minimize errors at the major code transitions.

5.2 18-bit ADC

While this satisfies the requirements for a DAC check standard, there remained a need to provide similar quality control for ADC testing. In particular, it must be verified that the transition-locking feedback loop in fact produces an input voltage whose average value, as measured by the remaining test set circuitry, is exactly equal to the defined transition level. These assumptions are not tested when calibrating DAC's alone. Again, commercially available ADC's are not adequately well behaved for this task.

To provide a check standard for the ADC operating mode, DAC-18 is combined with a precision analog comparator (developed at NBS for this purpose by H. K. Schoenwetter [9]) to create a precision, simulated ADC. The instrument is shown in simplified form in figure 10. For simplicity of discussion, it is represented as it would be implemented if offset binary coding rather than sign-magnitude were used for the reference codeword. So far as the test set is concerned, the instrument behaves exactly as would an 18-bit test ADC. However, unlike a true ADC, the instrument cannot accept an arbitrary input signal and provide a digital encoding of it. Instead, the simulation ADC must first be provided a "cue" in the form of the digital reference codeword used by the test set.

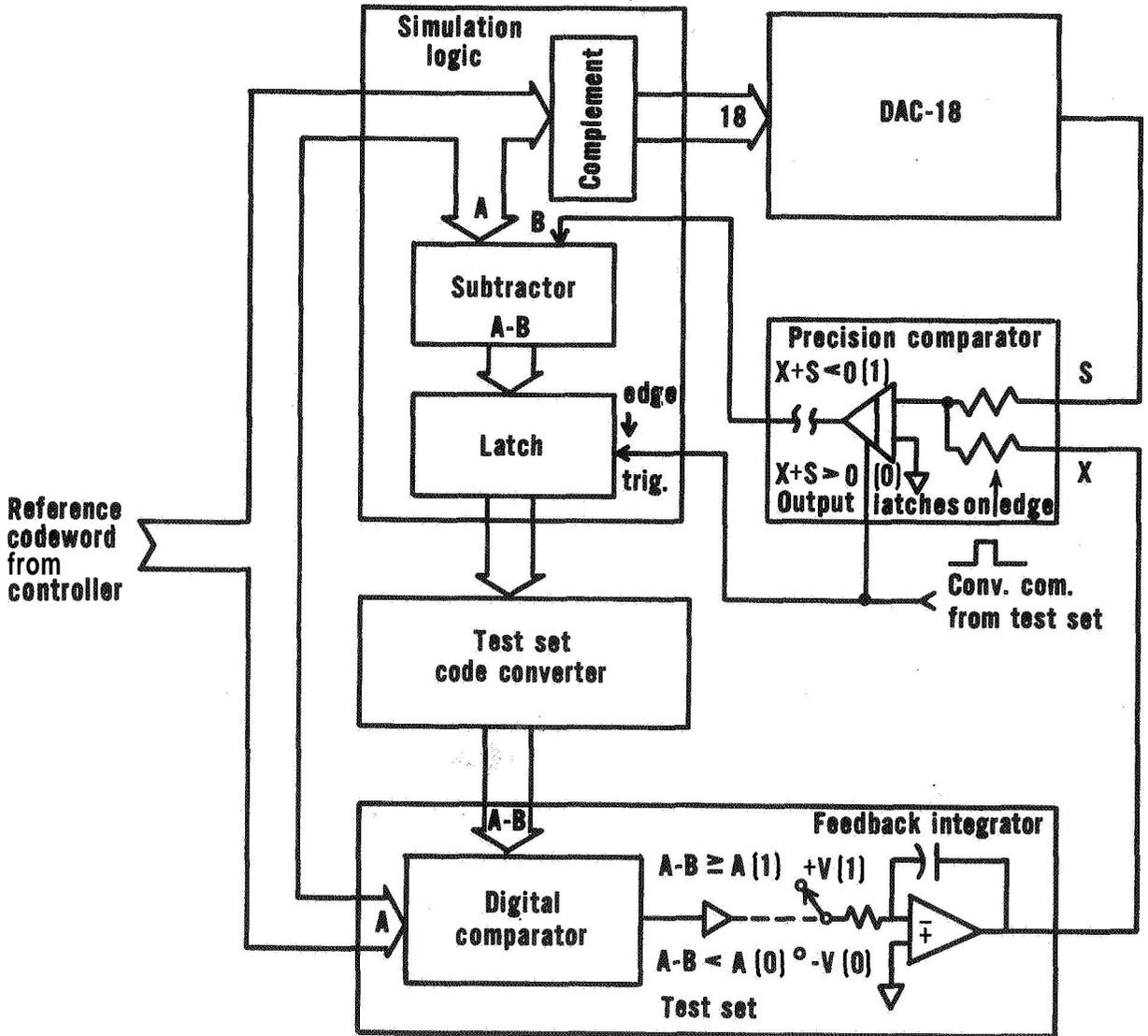


Figure 10. Simulation ADC and its connection to test set

This information instructs DAC-18 to output a corresponding (inverted) voltage S which is then compared to the input voltage from the test set X , by means of the precision comparator. The digital output of the comparator (0 or 1) is then subtracted from the reference **codeword** (A-B), and the result is taken to be the encoded output of the simulation ADC. This output is equal to the reference **codeword** when the input voltage is greater than DAC-18's (inverted) output ($X > S$), and is 1 LSB lower when the input is less than DAC-18's (inverted) output ($X < S$). As in testing any ADC, the test set accepts this output **codeword** and routes it through the code converter to the digital comparator controlling the feedback loop. Since the feedback loop locks on to the transition whose upper code is the reference codeword, any ADC output equal to the reference codeword, i.e., occurring when the analog comparator's output is zero, will cause the input voltage to decrease. Similarly, when the analog comparator outputs a "1," the simulated ADC output will be less than the reference codeword, and the input voltage will increase. Therefore, the feedback loop is exercised normally, and the input voltage seeks and maintains the transition level corresponding to the reference codeword. The accuracy of this level is determined by DAC-18 and the precision analog comparator. Since only one analog comparison need be made per conversion, the time available for the comparator to reach a decision is considerably longer than would be available if a full successive approximation routine were used. This additional time permits a more accurate decision to be made, and accordingly, the simulation ADC is capable of higher accuracy. Critical specifications of the precision comparator follow:

Input Impedance:	~5K Ω
Response Time:	30 μ s to within 10 μ V, following input steps up to 20V
Noise:	8 μ V rms referred to signal input
Offset:	Adjustable to zero; less than 8 μ V change (referred to input) under worst case dynamic conditions

Linearity Error: <0.4 ppm (input vs reference voltage) under worst case conditions. Temperature coefficient less than 0.2 ppm/°C.

Digital Circuits: Following a strobe pulse, the digital output is retained until the next strobe pulse. Opto-isolators provide isolation from the analog circuits.

6. TEST PROGRAMS AND PROCEDURE

After a test converter has been connected to the test set, energized, and determined to be operating properly, its input is set to positive full-scale and it then undergoes a warm-up period, continuing until the measurement drift is less than 0.1 LSB per 5 minutes. If large offset and gain errors are present, they are effectively reduced by performing an AOG correction routine unless they exceed the dynamic error measurement range of the test set. When excessive, they are manually trimmed, assuming that trim circuits have been made available and that such adjustments have been authorized by the customer.

As discussed previously, the input or output voltage is normally measured by averaging over a 16.7 ms period (one power line cycle). Under special circumstances, this period can be doubled. For the highest resolution converters (16 and 18 bits), five measurements are made and averaged for each code tested. This procedure effectively improves the measurement resolution from 1 ppm to 0.2 ppm.

6.1 Basic Linearity Test

For the basic linearity test, the 1024 codewords formed from the 10 most significant bits are tested in numerically ascending order. If the unit-under-test is an ADC, these reference codewords designate the upper codes of digital transitions, so that the measured input voltage corresponds to the transition between the designated codeword and the adjacent codeword below it. The chart (table 4) below indicates the test code sequences for both DAC's and ADC's, configured for both bipolar and unipolar operation. Note that the negative-most transition is designated by the reference code 000000000---1. Since no ADC transition exists for a reference code of all zeros, the next higher code is chosen instead. For simplicity, this convention is maintained for DAC's as well.

MSB										LSB				
1	2	3	4	5	6	7	8	9	10	11	N	
0	0	0	0	0	0	0	0	0	0	0	.	.	0	1
0	0	0	0	0	0	0	0	0	1	0	.	.	.	0
0	0	0	0	0	0	0	0	1	0	0	.	.	.	0
0	0	0	0	0	0	0	0	1	1	0	.	.	.	0
				:										
				:										
				:										
1	1	1	1	1	1	1	1	1	1	0	.	.	.	0

Table 4. Test code sequence, assuming straight binary or offset binary coding. Comparable codes are used for converters having other coding formats.

At each code the test set automatically measures the errors, defined as the difference between the input (output) of the ADC (DAC) under-test and the output of the reference DAC-20. Errors in DAC-20 are assumed to be negligible. These measured errors are numerically corrected for offset and gain, forcing the first and last code errors to zero. This is accomplished with the following calculations:

$$\epsilon_n^i = \epsilon_n - \epsilon_0 - (\epsilon_{1023} - \epsilon_0) \frac{n}{1023} \quad (4)$$

- where ϵ_n^i is the offset and gain corrected error at the n^{th} code
- ϵ_n is the measured error at the n^{th} code
- n is the code index
- ϵ_0 is the measured error at the negative-most code
- ϵ_{1023} is the measured error at the positive-most code, i.e., with bits 1-10 at logic "1."

The resulting values ϵ_n^i are the linearity errors of the converter-under-test and are recorded. These data are numerically processed to determine the maximum, minimum, and rms errors of the 1024 tested codes, and to determine, on a least-squared basis, individual correction coefficients for the 10 most significant bits.

6.1.1 Walsh Function Analysis

The correction coefficients just mentioned are derived from the Walsh function expansion of the test converter's error data. In this analysis, the set of error data derived from the basic linearity test is taken to represent a uniformly sampled function having a period of 2^N samples, where N , in this case, is 10. Walsh functions are a set of complete orthogonal functions capable of representing, by simple series, essentially any such function on a finite interval [10]. Such a series is analogous to a Fourier series, differing primarily in that Walsh functions are square-like rather than sinusoidal. Three properties of Walsh functions make them particularly useful in analyzing converter errors:

1. Walsh functions are orthogonal, and as such, each function of the series independently minimizes the mean-squared error in the representation of the original function.
2. Walsh functions are square-like, and assume a value of plus or minus one.
3. The set of 2^N Walsh functions contains a subset of N Rademacher functions which are exact square waves having periods of 2^n samples, where n ranges from 1 to N . This relationship is illustrated in figure 11, for $N=3$.

By applying property 3, it can be seen that the Rademacher functions have the same periodicity as the individual bits in a linearly ascending digital ramp as shown in figure 11. If the on and off states of a bit are defined as +1 and -1, respectively, then by property 2, for $N=10$, the 10 Rademacher functions exactly describe the digital states of the 10 bits tested in the 1024-point linearity test described above.

Finally, property 1 implies that the individual Rademacher coefficients will give the errors associated with each respective bit in the sense of the best (least-squared error) fit, independent of bit interaction or superposition error. Therefore, if no superposition error is present, a set of 10 Rademacher functions will completely describe the linearity errors of a 10-bit converter. Furthermore, if superposition errors are present, the 10 coefficients still describe the best corrections which can be applied to each individual bit when such corrections are considered over the entire range of code states. If such corrections based on the Rademacher coefficients were applied, the remaining (superposition) errors would have the minimum possible mean-squared value based on any method of individual-bit adjustments. In such cases where superposition errors are present, the remaining mean-squared error can, of course, be further reduced by the inclusion of additional Walsh coefficients beyond the Rademacher series. Of particular interest is the 0th Walsh coefficient, which by analogy to the DC component in Fourier analysis, provides the net offset or average value of the data set. Note that since the linearity errors are by definition zero at the endpoints,

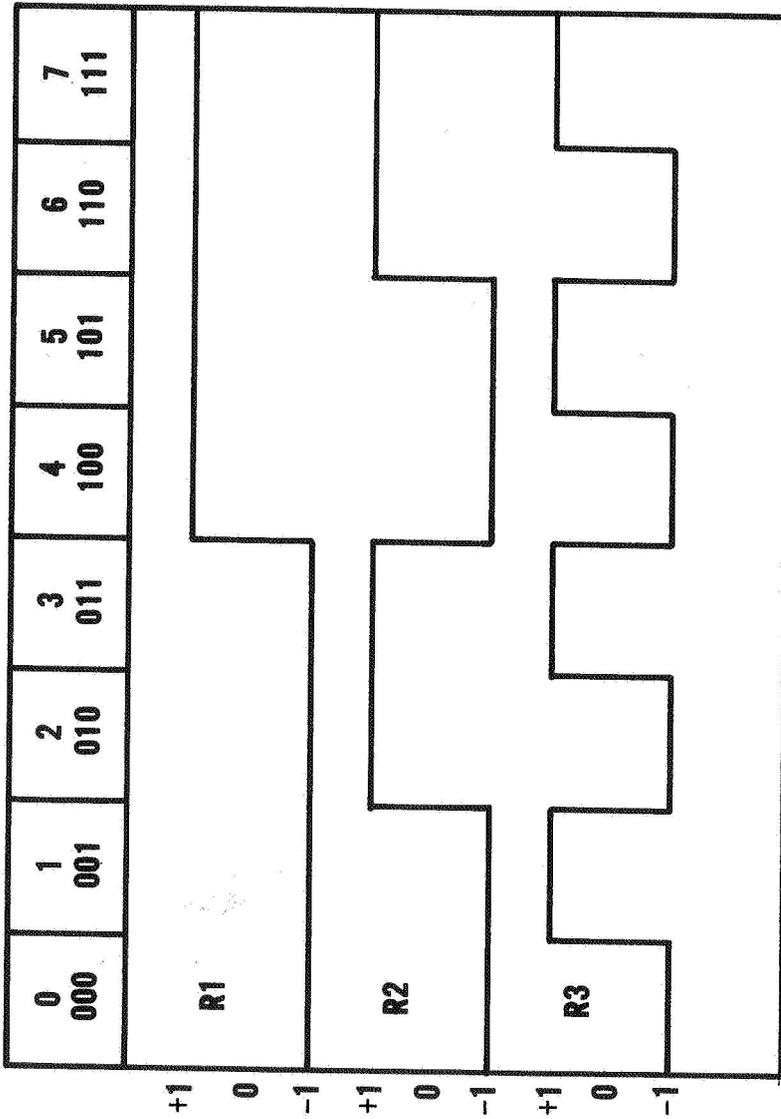


Figure 11. Periodicity of first three Rademacher functions

a net offset in the error data can occur only through the presence of superposition errors. While other Walsh coefficients could also be considered, usually only the 0th Walsh and the N Rademacher coefficients have an easily recognizable physical significance. And even for these coefficients, the significance is lost for certain converter types. For example, a flash-type ADC having 2^N-1 independent threshold circuits would be unlikely to exhibit significant correlation between linearity errors and the Rademacher series. Nevertheless, many ADC types, including successive approximation, and almost all DAC types will profit by this type of analysis.

The formulas used to calculate the rms error as well as the 0th Walsh and N(ten) Rademacher coefficients are as follows:

$$\text{rms error} = \sqrt{\frac{1}{1024} \sum_{n=0}^{1023} (\epsilon'_n)^2} \quad (5)$$

$$C_0 = \frac{1}{1024} \sum_{n=0}^{1023} \epsilon'_n \quad (6)$$

$$C_M = \frac{1}{1024} \sum_{n=0}^{1023} \epsilon'_n (2^{K_{Mn}} - 1) \quad (7)$$

where ϵ'_n is the linearity error of the nth code as defined previously

C_0 is the 0th Walsh coefficient or the average of errors ϵ'_n

C_M is the Mth Rademacher coefficient, or the correction coefficient for the Mth bit

K_{Mn} is the logic value of the Mth bit in the nth codeword. It has a value of either 1 or 0.

As the preceding discussion suggests, the determination of selected Walsh coefficients can indicate the extent to which superposition errors are present.

To determine the superposition errors from the correction coefficients, the coefficients are transformed back to a function of the original form, reconstructing the data set. The differences between the

measured and reconstructed data are then, by definition, the converter's superposition errors. The reconstruction is calculated with the following formula:

$$\epsilon_{Rn}^i = C_0 + \sum_{M=1}^{10} C_M(2^{K_{Mn}} - 1) \quad (8)$$

where ϵ_{Rn}^i is the reconstructed error for the n^{th} codeword.

Superposition errors are then defined as

$$\epsilon_{sn} = \epsilon_n^i - \epsilon_{Rn}^i, \quad (9)$$

and a superposition "figure of merit" is given by the rms value of ϵ_{sn} computed over the set of n codewords:

$$\text{rms}_s = \sqrt{\frac{1}{1024} \sum_{n=0}^{1023} (\epsilon_{sn})^2} \quad (10)$$

This information can uncover inherent design problems which cause effective coupling between bits, for example. In general, superposition errors establish a practical limit to the accuracy attainable with a given converter, beyond which no simple adjustments or corrections will be useful. If, however, the superposition errors are significantly lower than the measured linearity errors, then substantial improvement in performance might be possible through simple application of the correction coefficients, either by direct adjustment or via system software. Figure 12 presents plots illustrating two converters having, respectively, (a) small superposition errors, and (b) relatively large superposition errors.

The basic linearity test program is capable of plotting, vs digital codeword, all 1024 points each of error data, reconstructed error data, and superposition errors. The maximum, minimum, and rms errors of these data sets are each determined and printed on the plots, as are the 11 error coefficients. Provision is also made for presenting the measured errors or the superposition errors as a histogram in which the probability distribution of errors is more evident.

BIT COEFFICIENTS (LSB'S)

2.	-0.872
1.	0.474
2.	-0.155
3.	-0.257
4.	-0.126
5.	0.028
6.	0.042
7.	0.006
8.	0.000
9.	-0.028
10.	0.027

Date: MARCH 25, 1981
 Converter model tested: 14-BIT DAC
 Voltage Range: +/- 10 V
 Resolution: 14
 Polarity: BIPOLAR
 Bits tested: MSB
 Temp. 25

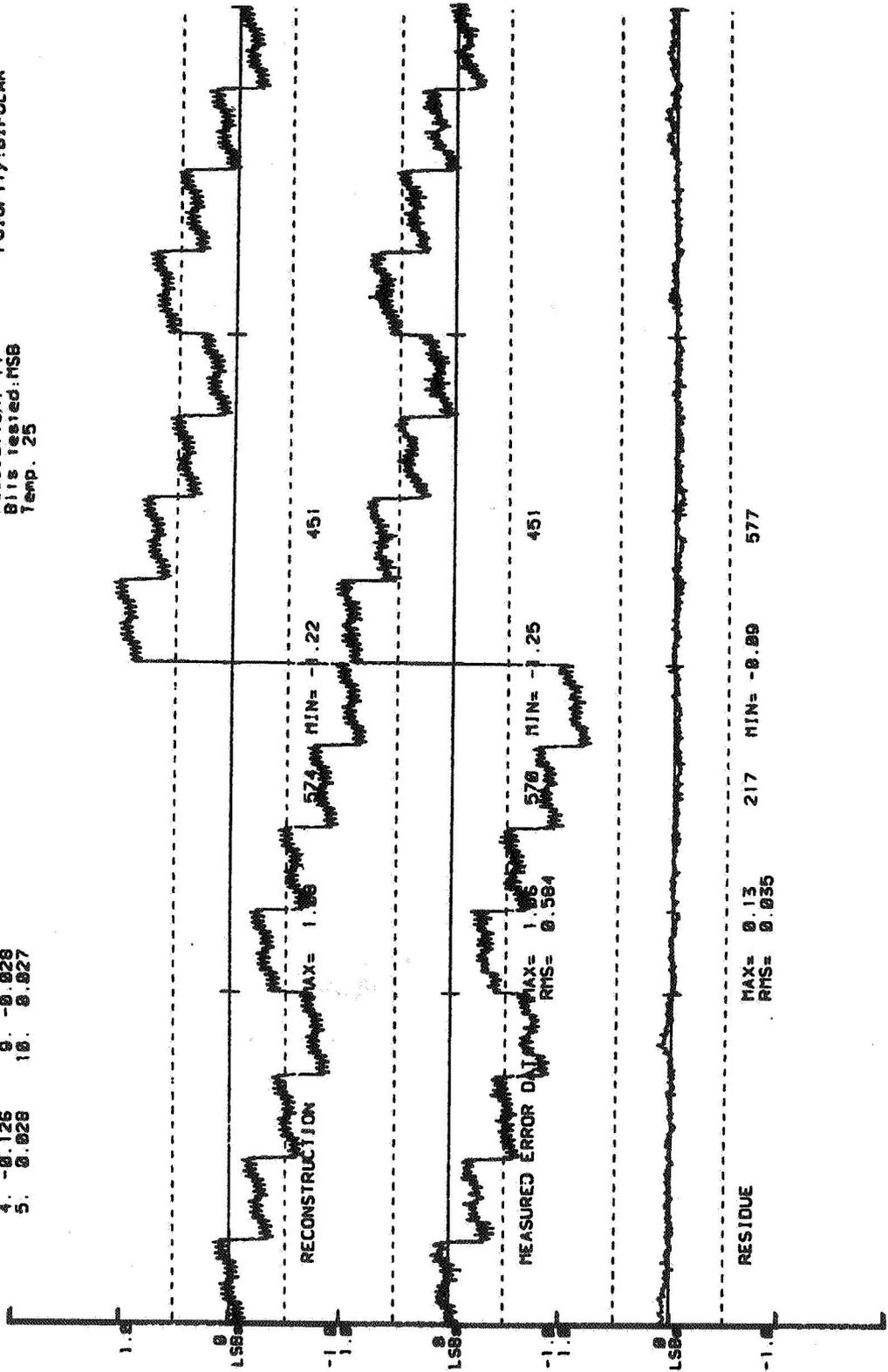


Figure 12(a). Linearity error data for converter having low superposition errors (14-bit DAC)

6.1.2 Analysis of Less Significant Bits

In the preceding discussion on the measurement and analysis of linearity errors, it is tacitly assumed that errors contributed by bits less significant than the 10th are negligible. This assumption is important, since it permits an abbreviated, less time-consuming test to be performed. Since it is important to assess this assumption, provision has been made to test all the least significant bits in like fashion. As a matter of convention, these bits are tested on either side of the major code transition, in the following code sequence:

MSB		LSB
1 2 3 4 5 6 7 8 9 10	11 . . . N	
0 1 1 1 1 1 1 1 1 1	1	0 . 0 0 0
0 1 1 1 1 1 1 1 1 1	1	0 . 0 0 1
0 1 1 1 1 1 1 1 1 1	1	0 . 0 1 0
.		
.		
0 1 1 1 1 1 1 1 1 1	1	1 . 1 1 1
1 0 0 0 0 0 0 0 0 0	0	0 . 0 0 0
1 0 0 0 0 0 0 0 0 0	0	0 . 0 0 1
1 0 0 0 0 0 0 0 0 0	0	1 0 . 0 1 0
1 0 0 0 0 0 0 0 0 0	0	1 . 1 1 1

Table 5.

In a manner quite similar to that just discussed, the individual bit coefficients and the related superposition errors are calculated. Generally, these determinations serve only to verify earlier assumptions and the results are not specifically included in the test report. Small errors which may be contributed by these less significant bits in the general operation of the converter are included in estimates of the random error of the measurement process. This contribution is considered more fully in the following section.

6.2 Random Code Test

While the test of linearity errors discussed in the previous section is based on a large number of data points, practical constraints generally make it impossible to cover all possible codes, much less all code sequences. The potential complexity of these untested residual error sources suggests that they be estimated instead by statistical

means, and be included in the estimate of the random error associated with the reported data. For this purpose, a random code test has been developed, and is applied to each converter-under-test.

In this test, test vectors are randomly selected from the full set of 2^N possible codewords, and 1024 of these are tested in succession. Each codeword has the full word length of the unit-under-test, so that the less significant bits are randomly included as well as the 10 most significant bits. The measured errors are again corrected for offset and gain, using the same endpoint test codes as are used in the basic linearity test (see table 4). The resulting random code linearity errors are sorted into 1024 possible bins according to the first 10 bits of each codeword. In this manner, it is possible to relate each random codeword error to one of the 1024 ordered errors measured in the basic linearity test. Note that, since the codewords are randomly selected, not all 1024 bins will be filled; in fact, it can be shown that an average of approximately 377 bins will remain empty. When the set of errors measured in the basic linearity test is subtracted from the sorted set of random code errors (ignoring bins that are not filled), then there remains a set of residual errors. These residuals are comprised of errors from several sources. First is the error contribution attributable to the less significant bits, and their possible interactions with the more significant bits. Second are the effects due to a random test sequence as opposed to a well ordered, linear sequence. Internal thermal effects might be prominent among these. Finally, there will be included other random errors of the measurement process which limit precision even when the same test sequence is repeated. Taken together, these effects give the residual errors a random appearance, and for simplicity, they are treated as being random. Accordingly, the rms value of the set of approximately 647 residual errors is calculated, and this value is taken to be an overall measure of the random error of the calibration process. This figure is used in determining the uncertainty limits that are stated in the calibration report. Results of a typical random code test are plotted in figure 13, where the top, middle, and bottom plots show, respectively, basic linearity errors, random code errors, and residual errors.

6.3 Differential Linearity Test

By definition, differential linearity errors (DLE's) are the errors in separation between adjacent code levels. Consequently, DLE's are associated with the discontinuities observed in the plots of linearity error vs codeword: the greater the discontinuity, the larger the DLE at that location. Assuming as before that the bits less significant than the 10th contribute insignificant errors, then the differential linearity errors for a particular converter can be easily determined by inspection from the plots of linearity error. Since the major discontinuities almost always occur at major transitions, an abbreviated test can provide actual measurements of the DLE's at the codes for which the errors are likely to be greatest. The following sequence of $2(N-1)$ codeword pairs is used for this test:

1024_RANDOM_CODE_TEST

DATE: MARCH 26, 1981
MODEL: 14-BIT ADC

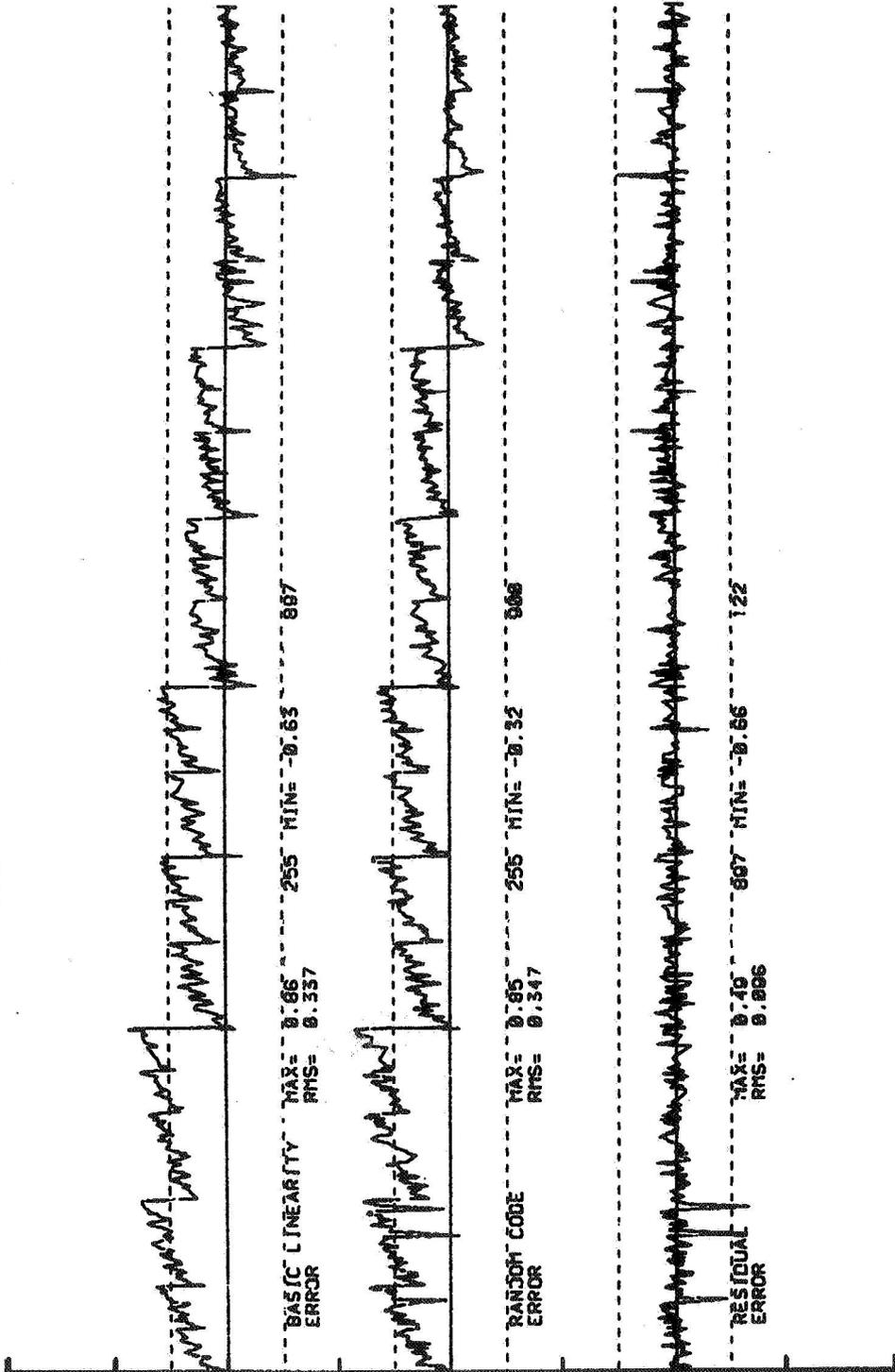


Figure 13. Typical results of random code test: Linearity error (1 LSB/DIV) versus output code (minus full scale to plus full scale)

MSB	LSB
1 2 3 N	N
{ 0 0 0 . . . 0 0 1	
{ 0 0 0 . . . 0 1 0	
{ 0 0 0 . . . 0 1 1	
{ 0 0 0 . . . 1 0 0	
: :	
{ 0 1 1 . . . 1 1 1	
{ 1 0 0 . . . 0 0 0	
{ 1 0 1 . . . 1 1 1	
{ 1 1 0 . . . 0 0 0	
: :	
{ 1 1 1 . . . 0 1 1	
{ 1 1 1 . . . 1 0 0	
{ 1 1 1 . . . 1 0 1	
{ 1 1 1 . . . 1 1 0	
{ 1 1 1 . . . 1 1 0	
{ 1 1 1 . . . 1 1 1	

Table 6

Differential linearity errors at each of the code pairs are simply computed as

$$\epsilon_{DL} = \epsilon_2 - \epsilon_1 \tag{11}$$

where ϵ_2 and ϵ_1 are the measured errors at the 2nd (higher) and 1st (lower) codes, respectively, of the code pair.

These errors are presented in tabular form with the respective **codeword** pairs designated by the higher **codeword** of each.

6.4 ADC Noise Test

As described in section 4.2, the measurement of equivalent rms input noise of ADC's relies on a theoretical relationship between input noise a and a reversal probability P associated with the transition-locking feedback loop. Two general assumptions concerning the noise characteristics have been made in the derivation of this relationship: that the

noise has a Gaussian distribution, and at the given sampling rate (10 kHz), successive values are uncorrelated. Since the noise measurements cannot be considered valid if the assumptions are incorrect, a simple test is used to verify the model. Figure 4 graphically presents the relationship between the ratio $\sigma/\Delta V$ and P , as predicted by the model. The validity of the model is tested for each test converter by determining the residuals after fitting the measured data to this relationship. The procedure is as follows: A random **codeword** is selected, and noise measurements are made at each of several values of ΔV set from the front panel. To reduce the standard deviation of each measurement, the average of 100 successive measurements of reversal probability P is taken for each setting of ΔV . Values of ΔV are chosen so that the ratios $\sigma/\Delta V$ fall roughly within the range 0.25-4. Assuming the rms noise remains constant over successive values of ΔV , two parameters are known for each measurement: the reversal probabilities P , and the relative values of $\sigma/\Delta V$, as ΔV is changed. If one value of $\sigma/\Delta V$ is normalized by applying the formula plotted in figure 4, the remaining values can be determined relative to this normalized point. In addition, the remaining values can also be computed by again applying the same theoretical **formula**. Significant differences between the two **determinations** indicate an invalid model. A figure of merit for the model is calculated from these differences as follows:

$$\sqrt{\frac{1}{N-1} \sum_{n=1}^N \left(\frac{\frac{\sigma'_n}{\Delta V_n} - \frac{\sigma}{\Delta V_n}}{\sigma/\Delta V_n} \right)^2} \quad (12)$$

where N is the number of measurement points (each made at a different value of ΔV).

$\sigma'/\Delta V_n$ is the value of $\sigma/\Delta V$ at the n th setting of ΔV , determined (by the first method) with respect to the normalized point.

$\sigma/\Delta V_n$ is the value of $\sigma/\Delta V$ at the n th point, determined by applying the theoretical formula to the measured probability P .

This expression gives the rms proportional error of noise values calculated from the model at successive values of ΔV , normalized to a fixed noise value.

Figure 14 illustrates this test. Five noise measurements each made at a different value of ΔV (10×2^{-14} , 10×2^{-15} , ..., $10 \times 2^{-18} V$), are plotted, together with the theoretical noise curve. One point, for which the measured probability was 0.83, has been normalized to the theoretical curve, **i.e.**, the plotted value of $\sigma/\Delta V$ was calculated from the theoretical formula. The remaining values have been plotted according to their known relationship to the normalized point, established by the relative

HYPOTHESES TEST FOR NOISE MEASUREMENT

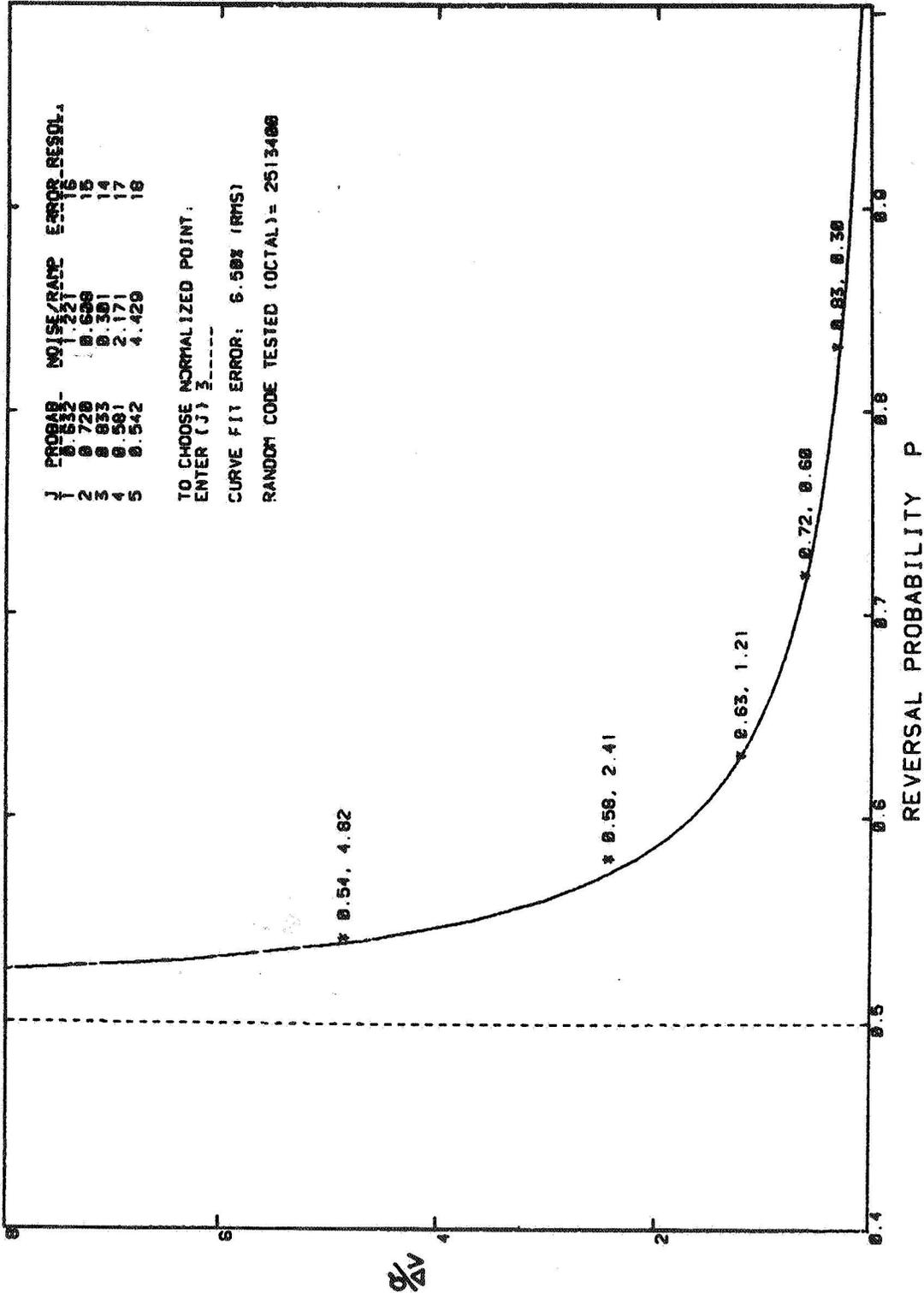


Figure 14. Hypotheses test for ADC noise measurement

values of AV which were selected. Next to each plotted point is printed its coordinates: the measured reversal probability, and the value of $\sigma/\Delta V$ determined from the normalized point. Note that, since AV changes by a power of 2 between points, the coordinates of $\sigma/\Delta V$ change accordingly. The "curve fit error," calculated from the figure of merit expression above, is printed in the upper right-hand corner.

Once the validity of the model has been demonstrated, either of two noise tests may be run: a determination of the average noise measured over 1024 random codes, or a test of noise vs code, measured and plotted at 64 randomly selected codes. In the average noise test, the 1024 reversal probabilities, each measured over the normal interval of 166 clock periods, are averaged. From this and the AV setting, the average, randomly sampled noise is computed. If the variation of noise with output code is desired, the second test may be run. For this test, the reversal probability is measured 100 times at each of 64 randomly selected codewords. The noise is calculated for each code from the average of the 100 measurements, and is plotted.

7. TEST SET CALIBRATION AND QUALITY CONTROL

To assure that the test set is performing within the tolerances set forth in table 2, several tests are periodically performed. The first four of these are designed to measure errors associated with components of the test system, e.g., the reference DAC, the error measurement circuitry, and the transition-locking circuit. The remaining tests employ the check standards described in section 5, and are intended to measure the overall system performance.

7.1 Reference DAC

The linearity of DAC-20 is quickly and easily measured and adjusted if necessary by employing the built-in self-calibration feature described in [6]. Independent verification of this self-calibration can also be performed using the technique described in the same reference. Self-calibrations of DAC-20 are performed no longer than a week prior to the calibration of 16- and 18-bit converters, or sooner if indicated by the results of check-standard tests.

7.2 Offset and Gain Errors

Although offset and gain errors of test converters are preferably measured directly (see sections 8.4 and 8.5), they can also be measured with the test set. For this, the offset and gain errors of DAC-20 and the test set's error measuring circuitry must be determined as well. For DAC-20, the offset and gain errors are measured in the same manner as for a test converter, as described in 8.4 and 8.5. The input offset of the test set is measured by shorting the analog inputs (reference and test) to ground, and recording the error data output from the test set. Equivalent gain error in the test set's error measuring circuitry results from

mismatch between the two input resistors. The gain error can be eliminated by swapping reference and test converter inputs to these two resistors, and taking the average of the error readings from both positions.

7.3 Accuracy of Error Measurement Circuitry

To determine the remaining measurement error after the input offset error has been removed, the test set can be calibrated directly against the less significant bits of DAC-20. The test is performed with the test set's "unknown" input open. A test program automatically exercises DAC-20's less significant bits in a digital ramp sequence, beginning at the equivalent offset binary code of

0 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0,

and sequentially incrementing the 20th bit until reaching the final code

1 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1.

The average of five error readings is taken from the test set at each code and recorded. Since the output error data is nominally direct reading in binary bits with the LSB having a weight of 2^{-20} , the output error code should ideally equal the nine least significant bits of DAC-20's input code. The nominal error range spanned is $-488 \mu\text{m}$ to $+487 \mu\text{m}$ in $0.95 \mu\text{m}$ increments. Deviations from ideal are easily computed by taking the difference between the two codes.

7.4 ADC Noise Measurement

The overall validity of the ADC noise measurement technique has been tested by applying well-characterized Gaussian noise from a noise generator to a second input of an ADC-under-test, and simultaneously to a wideband, true rms voltmeter [7]. For values of $\sigma/\Delta V$ in the range of 0.5 to 6, measurements of σ made with the test set and the rms voltmeter were in agreement to ± 10 percent or better. To verify that the characteristics of the noise to be measured fit the model, the test described in section 6.4 is performed. Finally, the following tests have been made of the noise introduced into the measurement from the test set itself:

1. Noise at the output of the integrating amplifier was measured directly, after shunting the feedback capacitor with a $10\text{K}\Omega$ resistor to prevent saturation. The measurement was made with the test converter removed.
2. The output noise was again measured directly, but under dynamic operating conditions with a low noise, 16-bit ADC in the test position. The value of ΔV was set to $10\mu\text{V}$, and the output was passed through a high pass filter with 10 kHz cutoff to reject low frequency fluctuations due to the response of the feedback loop.

3. Finally, the test set was used to measure the noise of the ADC check standard. Since the noise from the component parts, i.e., DAC-18 and the precision analog comparator, had been evaluated separately and the comparator's bandwidth was known, it was possible to estimate the additional noise contributed from the test set itself.

7.5 Overall System Performance

Overall system performance is monitored through periodic calibration of check standards. Until the test set's long-term stability can be determined, DAC-18 will be calibrated along with each 16-or 18-bit converter submitted for test, and will otherwise be recalibrated at one-month intervals. Because the ADC check standard's measured errors have not deviated significantly from DAC-18's, the ADC check standard will only be calibrated at six-month intervals. The results of typical linearity error measurements of the two check standards are shown, respectively, in figures 15 and 16. Note that in each case, the maximum measured error is less than the estimated systematic uncertainty reported in section 3. These check standard calibration records are kept on file, and the maximum and minimum measured errors of each are plotted against time for a convenient control chart. When the control chart indicates that the peak error is approaching the claimed systematic uncertainty, the check standard and DAC-20 will both be independently readjusted, using their respective self-calibration routines. A subsequent calibration will be performed to verify that the measured errors have been reduced to less than those claimed.

8. ERROR ANALYSIS

The estimated systematic uncertainties associated with each measured converter parameter have been listed in table 2 of section 3. The various component errors of which these are comprised are presented in the following subsections, together with their methods of estimation.

8.1 Linearity Error

Linearity error is computed from the measurements of ϵ_n , ϵ_0 and ϵ_{1023} , by applying equation (4). The estimated systematic uncertainty in each of these measured component quantities is taken to be the arithmetic sum of errors in DAC-20, the test set's error measurement circuitry, and for ADC's, the uncertainty in the location of transition levels. The total systematic uncertainty for linearity errors is computed as discussed below, using equation (4), from these individual uncertainties.

8.1.1 DAC-20

The estimated maximum linearity errors for DAC-20, when maintained at a constant temperature ± 0.5 °C, are as follows:

Range	Estimated Maximum Systematic Uncertainty	
	At measurement codes for ϵ_0 and ϵ_{1023}	All other codes
± 10 V	± 0.5 ppm	± 1.0 ppm
0-10 V, ± 5 V	± 0.75 ppm	± 1.5 ppm
0-5 V	± 1.0 ppm	± 2 ppm

These values assume a maximum conversion rate of 10/s, and a recalibration interval of 1 month.

Note that the estimated uncertainties for the codes at which ϵ_0 and ϵ_{1023} are measured (see table 4), are smaller than for other codes. These codes differ from the minus and plus full-scale endpoints only by the 10 least significant bits.

8.1.2 Error Measuring Circuitry

Based on measurements described in section 7.3, this circuitry is estimated to contribute a maximum error of $\pm(0.6 \text{ ppm} + 0.02 \text{ LSB})$, assuming that the least count quantization **uncertainty** has been reduced by taking the average of five readings per measurement. For converters of 14 bits and fewer, only one reading per measurement is taken. In this case, the maximum error is increased by 1 ppm.

8.1.3 ADC Feedback Loop Errors

Since AV is normally set to give a transition-locking precision of 1/16 LSB, an uncertainty of 0.063 LSB is assigned to this source. To this is added 1 ppm, estimated to be the maximum error resulting from transient voltage spikes introduced into the integrator's output via coupling through the input switch. These estimates are supported by tests of the ADC check standard.

8.1.4 Total Estimated Uncertainty

The combined estimated systematic uncertainties for each of the component measurements are as follows:

Estimates in (ppm + LSB)

Range	DAC's			ADC's		
	ϵ_n	ϵ_0	ϵ_{1023}	ϵ_n	ϵ_0	ϵ_{1023}
+ 10V	1.6+0.02	1.1+0.02	1.1+0.02	2.6+0.08	2.1+0.08	2.1+0.08
0-10V, +5V	2.1+0.02	1.4+0.02	1.4+0.02	3.1+0.08	2.4+0.08	2.4+0.08
0-5V	2.6+0.02	1.6+0.02	1.6+0.02	3.6+0.08	2.6+0.08	2.6+0.08

Applying equation (4), the total estimated systematic uncertainties in the measurement of linearity error are given by

$$\epsilon_n' = \epsilon_n + \epsilon_0 \left(1 - \frac{n}{1023}\right) + \epsilon_{1023} \cdot \frac{n}{1023} \quad (13)$$

where the ϵ 's now refer to the maximum uncertainties in each term.

The maximum value of this expression is given by the greater of $(\epsilon_n + \epsilon_0)$ or $(\epsilon_n + \epsilon_{1023})$. Therefore, the resulting total systematic uncertainties are as listed in table 2 of section 3.

8.2 Bit Coefficients

The estimates of maximum systematic uncertainty in the reported values of the 11-bit coefficients are based on the assumption that each of the 1024 measurements from which the coefficients are derived can have the same maximum uncertainty as estimated in 8.1.4. However, because the bit coefficients are derived from an averaging process (equations (6) and (7)), the 1/16 LSB uncertainty in an ADC transition location can be expected to become insignificant for the values ϵ_n . In addition, half of the data points ϵ_n are weighted by -1 for all coefficient determinations except the 0th (see equation (7)). Therefore, it is expected that the relatively constant 1 ppm feedthrough error (see section 8.1.3) for ADC's will also become insignificant. The uncertainties in the bit coefficients contributed by uncertainties in the terms ϵ_0 and ϵ_{1023} are given by the respective Walsh transform coefficients of the linear function $\epsilon_0 + (\epsilon_{1023} - \epsilon_0) \cdot \frac{n}{1023}$. It is easily shown that, to a close approximation, these are:

$$C_0 = \frac{\epsilon_{1023} + \epsilon_0}{2} \quad (14)$$

$$C_M = \frac{\epsilon_{1023} - \epsilon_0}{2^M} \quad M = 1-10 \quad (15)$$

where the C's are the resulting uncertainties in the respective bit coefficients, and the E's are the uncertainties in the respective measurements.

Therefore, the combined systematic uncertainties for the bit coefficients are given by the sum of the uncertainties in ϵ_n and the respective C coefficients above, ignoring the ADC transition location and feedthrough uncertainties where appropriate. The calculated results are given in table 2. For simplicity, the uncertainties in the higher bit coefficients are taken to be equal to the somewhat larger value for C_1 .

8.3 Differential Linearity Errors

Since DLE's are each determined from two measurements, ϵ_n and ϵ_{n-1} , the maximum systematic uncertainty is twice the uncertainty in one measurement of ϵ_n (listed on page 45).

8.4 Offset Error

In general, converter offset and gain measurements are not required, since it is common practice to provide adjustable trimmer circuits which are periodically set to suit individual system requirements. If, however, accurate voltage measurements directly traceable to legal standards are required, then such measurements can be provided. Offset errors are measured directly by setting the test converter to the designated code (the first in table 4), and measuring the input (or output) voltage by direct comparison with a transfer standard calibrated by the Electrical Measurements and Standards Division of NBS. The estimated maximum systematic uncertainty in this process is 3 ppm for DAC's, and 3 ppm + 0.07 LSB for ADC's.

8.5 Gain Error

Following the measurement of offset error (see section 8.4), gain error is measured similarly by setting the test converter to the last code listed in table 4, and measuring the corresponding voltage. Because the definition of gain is linked to offset, the two measurements must be combined to derive the gain error with consequent doubling of systematic uncertainties, i.e., 6 ppm and 6 ppm + 0.13 LSB, respectively, for DAC's and ADC's. It should be recognized, however, that the second voltage measurement can, if desired, be calculated from the offset and gain errors with a systematic uncertainty equal to that of a single measurement.

8.6 ADC RMS Input Noise

Significant systematic uncertainties in the measurement of rms input noise can arise from several sources:

1. Uncertainty in the value of A_V , which provides the reference voltage for the noise measurement. This is estimated to be $\pm (5\% + 10\mu V)$.
2. Magnitude mismatch between positive and negative values of A_V .
3. Deviation of noise characteristics from the ideal model.
4. Approximations in the mathematical expression of the relationship plotted in figure 4.
5. Noise introduced by the test set itself. This has been measured to be approximately $30\text{nV}/\sqrt{\text{Hz}}$ in the frequency range of 10 kHz to 1 MHz (see section 7.4). To establish the contribution of this noise source to the measured noise, the effective bandwidth of the test converter must first be known. Since this information is generally unavailable, the lower uncertainty limit is taken to be -100 percent, reflecting the uncertain noise contribution from the test set.

Of these uncertainty sources, 2-4 are all included in the model test described in section 6.4. Noise values will not be reported if the figure of merit (from equation (12)) for this test exceeds 15 percent. The upper bound of the estimated systematic uncertainty is taken to be the sum of this figure of merit limit and the $5\% + 10\mu V$ uncertainty in A_V . Therefore, the lower and upper bounds for the rms noise due to systematic uncertainty are, respectively,

$$0; \text{rms}_N + (20\% + 10\mu V),$$

where rms_N is the measured value.

9. CALIBRATION REPORTS

Sample calibration reports for both DAC's and ADC's are reproduced on pages 48-58. While the samples include all tests which will be offered on a routine basis, only those tests which are specified by the individual customer will be conducted and reported. The basic linearity test described in section 6.1 comprises the minimum test, to which others may be added at an additional fee, as described in NBS Special Publication 250.

On pages 59 and 60 are reproduced several Explanatory Notes for Data Converter Calibration Reports, which are included on separate sheets with each report,

U.S. Department of Commerce
National Bureau of Standards
Washington, D. C. 20234

Report of Calibration

Digital-to-Analog Converter, 14 Bit
(Manufacturer's name, model number)
(Serial number)

Submitted by
(Name and address)

This data converter was tested on January 14, 1981 at a temperature of 26 °C, on the + 10-volt range using offset binary coding. The tests were conducted in accordance with the methods described in NBS Technical Note 1145, "A Calibration Service for Analog-to-Digital and Digital-to-Analog Converters,"

■. Linearity Test

Linearity errors were measured at the 1024 codewords formed from the 10 most significant bits. These errors, plotted in figure 1(b), had the maximum, minimum, and rms values reported in table 1.

Table 1

	Error LSB's (Least Significant Bits)	Code Position (0-1023)
Maximum	0.99	588
Minimum	-1.05	459
RMS	0.49	---

Eleven individual correction coefficients corresponding to the average error and the 10 most significant bits have been computed from the error data on a least-squared error basis. These are given in table 2.

Table 2

Bit Correction Coefficients (LSB's)

0.	-0.018	6.	0.037
1.	0.405	7.	-0.003
2.	-0.143	8.	0.007
3.	-0.208	9.	-0.033
4.	-0.103	10.	0.022
5.	0.024		

Superposition errors (figure 1(c)) have also been calculated from the measured errors by subtracting the errors reconstructed from the reported bit correction coefficients (figure 1(a)). The maximum, minimum, and rms values of the superposition errors are given in table 3.

Table 3

	Superposition Error LSB's	Code Position 0-1023
Maximum	0.08	29
Minimum	-0.09	547
RMS	0.03	

The values reported in tables 1 and 3 and plotted in figures 1(b) and 1(c) are estimated to have a maximum systematic uncertainty of ± 0.09 LSB.

II. Differential Linearity

Differential linearity errors were measured at $2(N-1)$ pairs of adjacent codewords. The measured values are reported in table 4 where each pair is designated by the higher of the two codewords.

The estimated uncertainties given in this report apply to the measurements at the time and under the conditions specified and should not be interpreted as being indicators of the long-term stability of the converter.

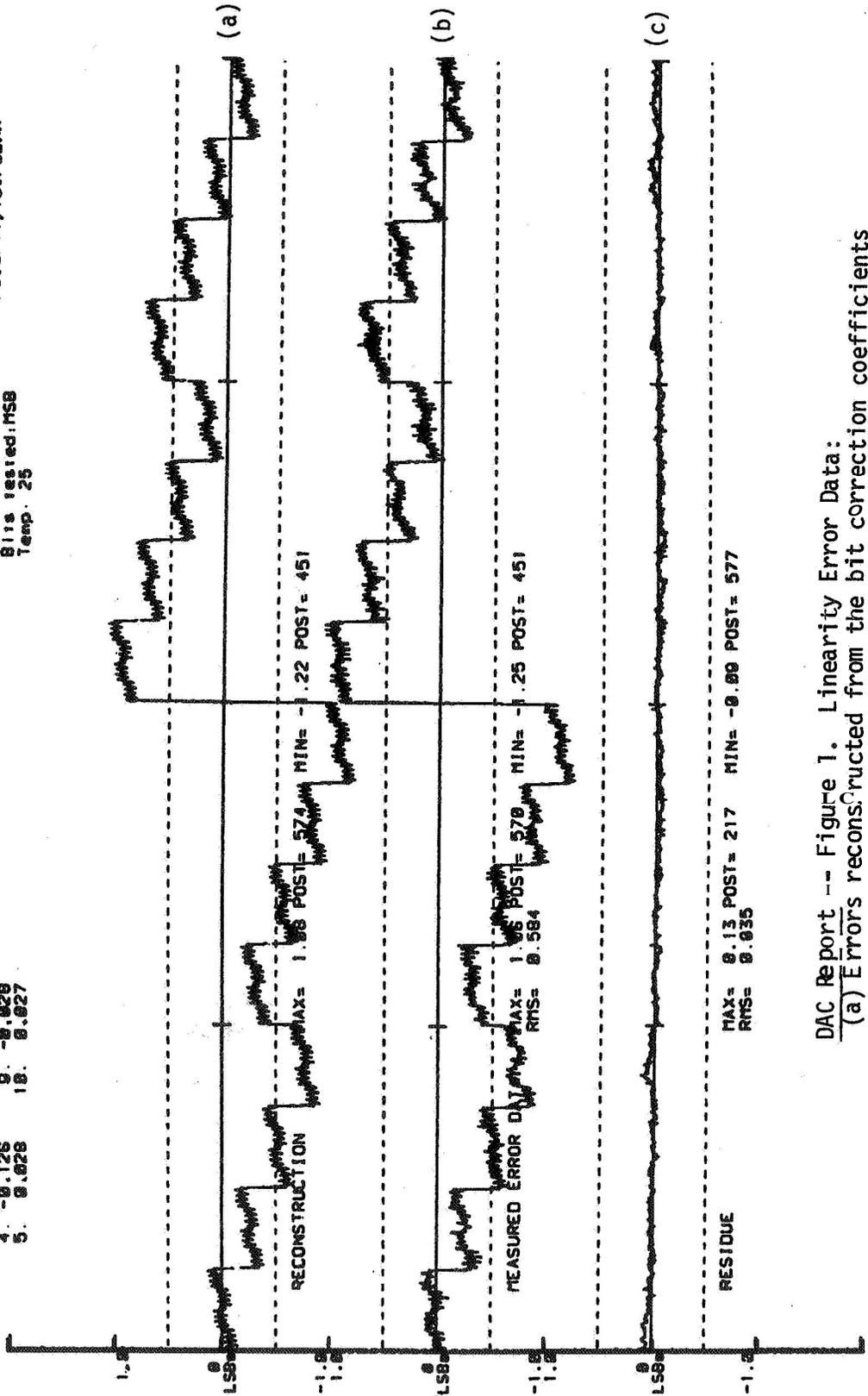
For the Director
National Engineering Laboratory

B. A. Bell
Electrosystems Division

BIT COEFFICIENTS (IN LSB'S)

- 0. -0.078
- 1. 0.474
- 2. -0.155
- 3. -0.257
- 4. -0.126
- 5. 0.028
- 6. 0.842
- 7. 0.886
- 8. 0.880
- 9. -0.829
- 10. 0.827

Date:
 Converter mode) tested:
 Voltage Range: +/- 10 V
 Resolution: 14
 Bits tested: MSB
 Polarity: BIPOLAR
 Temp. 25



DAC Report -- Figure 1. Linearity Error Data:

- (a) Errors reconstructed from the bit correction coefficients reported on second page of test report
- (b) Measured errors
- (c) Superposition errors (measured errors - reconstructed errors)

Report of Calibration

Analog-to-Digital Converter, 14 Bit
(Manufacturer's name, model number)
(Serial number)

Submitted by
(Name and address)

This data converter was tested on January 14, 1981 at a temperature of 26 °C, on the bipolar ± 10 -volt range using offset binary coding. For all tests, the conversion rate was 10^4 per second. The tests are conducted in accordance with the methods described in NBS Technical Note 1145, "A Calibration Service for Analog-to-Digital and Digital-to-Analog Converters." In this report, the levels at which the designated errors have been measured are the input levels at which the digital output transitions between adjacent codes occur. The transition levels are defined by the upper digital code of the transition in question.

I. Linearity Test

Linearity errors were measured at the 1024 codewords formed from the 10 most significant bits. These errors, plotted in figure 1(b), had the maximum, minimum, and rms values reported in table 1.

Table 1

	Error LSB's (Least Significant Bits)	Code Position (0-1023)
Maximum	0.83	255
Minimum	-0.65	897
RMS	0.32	---

Eleven individual correction coefficients corresponding to the net offset and the 10 most significant bits have been computed from the error data on a least-squared error basis. These are given in table 2.

Table 2

Bit Correction Coefficients (LSB's)

0.	0.218		
1.	-0.173	6.	0.051
2.	-0.094	7.	0.041
3.	0.025	8.	0.044
4.	0.057	9.	0.020
5.	0.064	10.	0.026

Superposition errors (figure 1(c)) have also been calculated from the measured errors by subtracting the errors reconstructed from the reported bit correction coefficients (figure 1(a)). The maximum, minimum, and rms values of the superposition errors are given in table 3.

Table 3

	Superposition Error LSB's	Code Position 0-1023
Maximum	0.16	513
Minimum	-0.32	897
RMS	0.07	

The values reported in tables 1 and 3 and plotted in figures 1(b) and 1(c) are estimated to have a maximum systematic uncertainty of ± 0.24 LSB.

II. Differential Linearity

Differential linearity errors were measured at $2(N-1)$ pairs of adjacent codewords. The measured values are reported in table 4 where each pair is designated by the higher of the two codewords.

IV. Equivalent RMS Input Noise

A. Average Noise

The equivalent rms input noise, when measured over 1024 randomly selected codes, had the following average value:

ms input noise: 122 μV

B. The equivalent rms input noise, measured at 64 randomly selected codes, is plotted in figure 2.

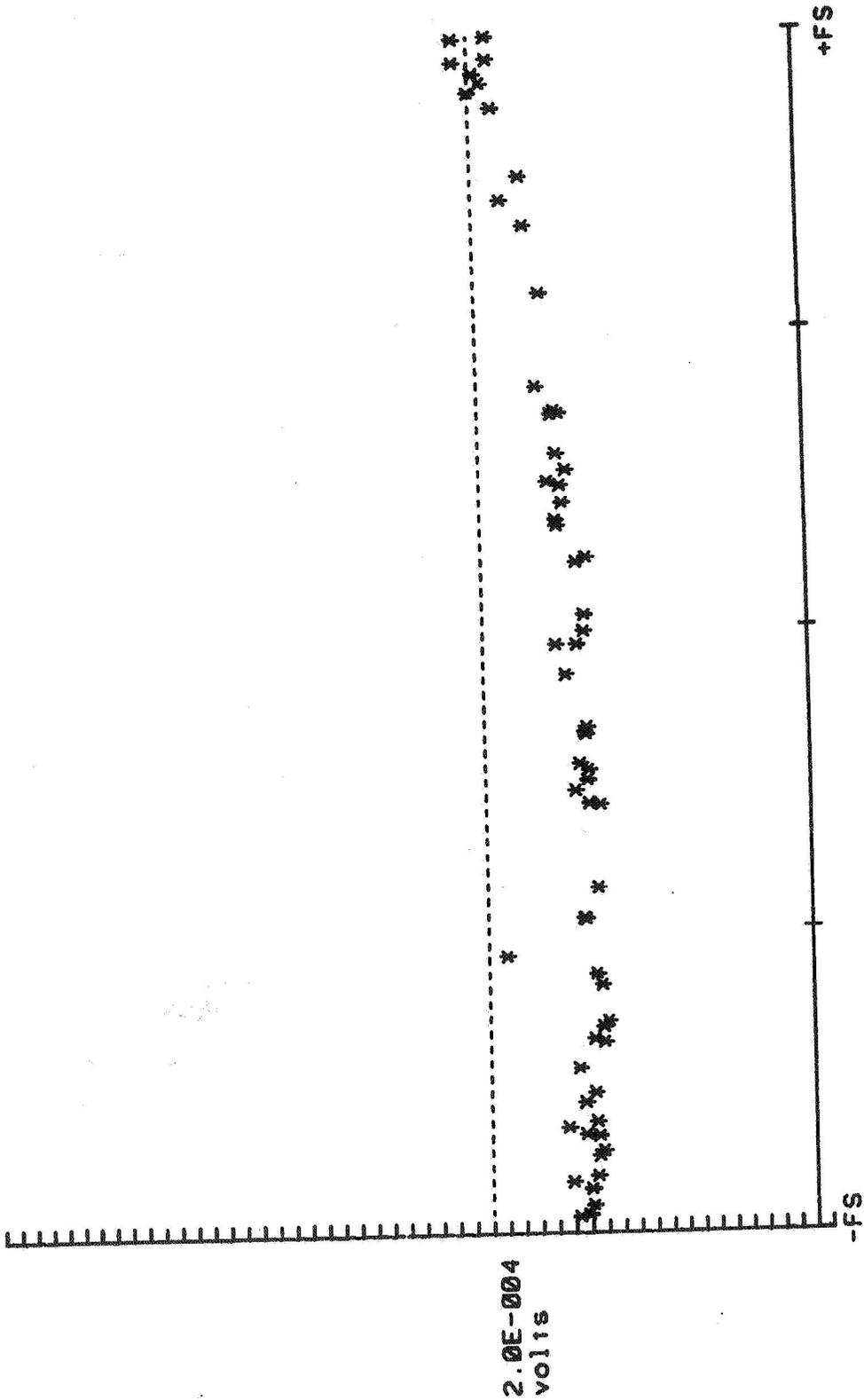
C. The true noise is unlikely to exceed the values reported in IV.A, and plotted in figure 2, by more than 35 μV . A lower limit to the reported values cannot be assigned since the bandwidth of the test converter is unknown. This figure includes allowances for both the random and systematic errors of the calibration process.

The estimated uncertainties given in this report apply to the measurements at the time and under the conditions specified and should not be interpreted as being indicators of the long-term stability of the converter.

For the Director
National Engineering Laboratory

B. A. Bell
Electrosystems Division

RANDOM CODE VS. AVERAGE OF 100 NOISE READINGS AT EACH CODE
Y-AXIS SCALE: $1.0E-5$ VOLTS PER UNIT
NUMBER OF RANDOM CODES: 64



ADC Report -- Figure 2. Equivalent rms input noise: measured noise versus output code

Explanatory Notes for Data Converter Calibration Reports

1. Test Code Sequence for Measurements of Linearity Errors

Codeword Position Number	Test Code, in equivalent binary or offset binary format											
	MSB										LSB	
	1	2	3	4	5	6	7	8	9	10	11	. . . N
0	0	0	0	0	0	0	0	0	0	0	0	. . . 0 1
1	0	0	0	0	0	0	0	0	0	1	0	. . . 0
2	0	0	0	0	0	0	0	0	1	0	0	. . . 0
3	0	0	0	0	0	0	0	0	1	1	0	. . . 0
.												
.												
1023	1	1	1	1	1	1	1	1	1	1	0	. . . 0

2. Error Definitions

Linearity Error: The difference between the actual and ideal levels of the static input/output characteristic after offset and gain errors have been removed.

Differential Linearity Error: The difference between the actual and the ideal separation between adjacent levels.

Offset Error: The difference between the actual and ideal levels, measured at the 0th codeword in (1) above.

Gain Error: The difference between the actual and ideal levels, measured at the 1023 codeword in (1) above, after removing offset errors.

Equivalent RMS Input Noise: The rms value of the effective internal noise of an ADC, referred to its input terminals.

In each of these definitions, the specified levels are the discrete output levels for DAC's, and for ADC's, they are the analog input levels at which the digital output transitions between adjacent codes occur. In the latter case, the transition levels are defined by the upper digital code of the transition in question.

3. Application of Bit Correction Coefficients

The 11-bit correction coefficients listed in the **calibration** report have been calculated from the 1024 measurements of linearity error plotted in figure 1(b) of the report. The first coefficient represents the net linearity error for the test converter, averaged over all codes. The remaining 10 coefficients represent the equivalent contribution of each of the first 10 bits, respectively, to the measured linearity errors. When applied according to the following formula, the 11

coefficients give estimates having minimum mean-squared uncertainty of the linearity error at any specified codeword.

$$\epsilon_n = C_0 + \sum_{m=1}^{10} C_m (2^{K_{mn}} - 1)$$

where ϵ_n is the estimated error at the n^{th} code

C_0 is the 0^{th} correction coefficient

C_m is the m^{th} correction coefficient

K_{mn} is the logic value of the m^{th} bit in the n^{th} codeword.
It has a value of either 1 or 0.

The errors in the values ϵ_n are the so-called superposition errors plotted in figure 1(c).

4. Random Code Test

While the linearity errors presented in section I were measured at a large number of test codes, time constraints make it impractical to cover all possible codes, much less all code sequences. Because of the potential complexity of these untested residual error sources, they have been estimated by statistical means. For this purpose, a random code test has been applied, in which test codes were randomly selected from the full set of 2^n possible codewords, and linearity measurements were made at 1024 of these codes in succession. Deviations in these random code errors from those predicted by the test results reported in section I were recorded, and their rms value was calculated. In many applications the residual errors can be considered random, and in these cases the calculated ms value is an estimate of their standard deviation. However, the residual errors also include systematic components attributable to the less significant bits, as well as to the differences between a random test sequence and a well-ordered, linear sequence. This calculated ms value can also be considered the maximum probably standard deviation of the random errors in the values reported in section I. For the errors reported in section II, the maximum standard deviation will be $\sqrt{2}$ times the calculated ms value since each determination of differential linearity error requires two measurements.

10. ACKNOWLEDGMENTS

The authors wish to acknowledge the substantial contribution made by Thick Wong to the development and documentation of the software supporting the calibration system.

11. REFERENCES

- [1] Tewksbury, S. K., et al. Terminology related to the performance of S/H, A/D, and D/A circuits. *IEEE Trans. Circuits Syst.*, Vol. CAS-25; 1978 July.
- [2] Naylor, J. Testing digital/analog and analog/digital converters. *IEEE Trans. Circuits Syst.*, Vol. CAS-25; 1978 July.
- [3] Sheingold, D., ed. Analog - digital conversion handbook. Norwood, MA: Analog Devices, 1972.
- [4] Havener, R. Catch missing codes. *Electron. Des.*; 1975 August.
- [5] Corcoran, J. J., et al. A high-resolution error plotter for analog-to-digital converters. *IEEE Trans. Instrum. Meas.*, Vol. IM-24; 1975 December.
- [6] Souders, T. M. and Flach, D. R. A 20-bit+sign, relay switched D/A converter. *Nat. Bur. Stand. (U.S.) Tech. Note* 1105; 1979 October.
- [7] Souders, T. M. and Lechner, J. A. A technique for measuring the equivalent rms input noise of A/D converters. *IEEE Trans. Instrum. Meas.*, Vol. IM-29; 1980 December.
- [8] Schoenwetter, H. K. A high-speed low-noise 18-bit digital-to-analog converter. *IEEE Trans. Instrum. Meas.*, Vol. IM-27; 1978 December.
- [9] Schoenwetter, H. K. A sensitive analog comparator, to be published as *Nat. Bur. Stand. (U.S.) Tech. Note*.
- [10] Walmsley, W. M. Walsh functions, transforms and their application. *Electronic Eng.*; 1974 June.

APPENDIX A

Test Board Preparation and Documentation

Each data converter submitted for calibration must be suitably mounted on a test board and wired to a pair of standard connectors, following the pin-function designations presented in sections I and II below. The converter board must hold all circuitry necessary for stand-alone operation, including a voltage reference, and for DAC's, an output amplifier. Before shipping to NBS, the boards should be tested to insure the wiring is correct and the converter is operating properly. Appropriate documentation should also accompany each converter, including the manufacturer's description and specification sheets, and additional information pertaining to the test board. The following items must be included:

- Voltage range
- Coding format
- Resolution (in bits)
- Conversion time (for ADC's)
- "Status" line and "convert command" timing
- Input impedance (for ADC's)

If trimming circuits for offset and gain are provided, it should be stated whether or not NBS is authorized to adjust their settings. When authorization is given, the manufacturer's recommended trimming procedure should be included.

Either printed circuit board edge connectors or D type subminiature connectors may be used for interfacing to the NBS calibration facility. These are discussed in the following sections.

I. Printed Circuit Board Edge Connectors

Figure A-1 shows the printed circuit board edge connector option for interfacing to the calibration facility. Table A-1 gives the contact assignments for connectors J1 and J2. In general, board dimensions should not exceed 8 x 10 inches (20 x 25 cm). Contacts for both connectors J1 and J2 are 0.090 inches (2.3 mm) wide on 0.156 inch (4.0 mm) centers. Board thickness is 0.062 inches (1.57 mm).

II. D Type Subminiature Connectors

Connections may also be made to the calibration facility using the D subminiature series of connectors. Two of these are needed, a 25-pin socket and a 9-pin socket. The pin designations are given in table A-2. Contact size is #20.

Table A-1

22/44 Contact Printed Circuit Board Edge Connector Designations

Connector J1

Contact	Function	Contact	Function	
A	Bit 1 MSB	1	NC	
B	2	2	Convert command	
C	3	3	NC	
D	4	4	Status (ADC's)	
E	5	5		
F	6	6		
H	7	7		
J	8	8		
K	9	9		
L	10	10		
M	11	11		NC
N	12	12		
P	13	13		
R	14	14		
S	15	15		
T	16	16		
U	17	17		
V	Bit 18 LSB	18		
W	NC	19		
X	NC	20		
Y	Logic Ground	21	Logic Ground	
Z	+ 5 volts	22	+ 5 volts	

Connector J2

A	Analog Signal (ADC input or DAC output)	1	Analog Signal Common
B	NC	2	NC
C	NC	3	NC
D	Analog Supply Common	4	Analog Supply Common
E	+ 15 volts	5	+ 15 volts
F	- 15 volts	6	- 15 volts

Table A-2

D Subminiature Connector Pin Designations

25 Pin Socket		9 Pin Socket	
Pin	Function	Pin	Function
1	Bit 1 MSB	14	14
2	2	15	15
3	3	16	16
4	4	17	17
5	5	18	18 (LSB)
6	6	19	NC
7	7	20	NC
8	8	21	Status (ADC's)
9	9	22	NC
10	10	23	Convert Command
11	11	24	+ 5 volts
12	12	25	Logic Ground
13	13		

III. General

A. NBS power supply voltage tolerance and output current capability:

+15 V	+ 300 mV/-0 mV,	100 mA output
-15 V	- 300 mV/+0 mV,	100 mA output
+5 V	+ 50 mV/-50 mV,	1000 mA output

B. "Status" Line

The "status" output for ADC's indicates whether or not a conversion is in progress. It must be specified which logic level (high or low) corresponds to "conversion in progress."

C. Convert Command

The "convert command" supplied by the NBS test facility is a positive going pulse of 2 μ s duration. DAC boards which do not include input data latches will probably not require a convert command. All ADC's must be connected so that each conversion is initiated by this externally supplied command.

D. Special Interfaces

Connector types or arrangements other than those specified in sections I and II may only be used by special arrangement with NBS.

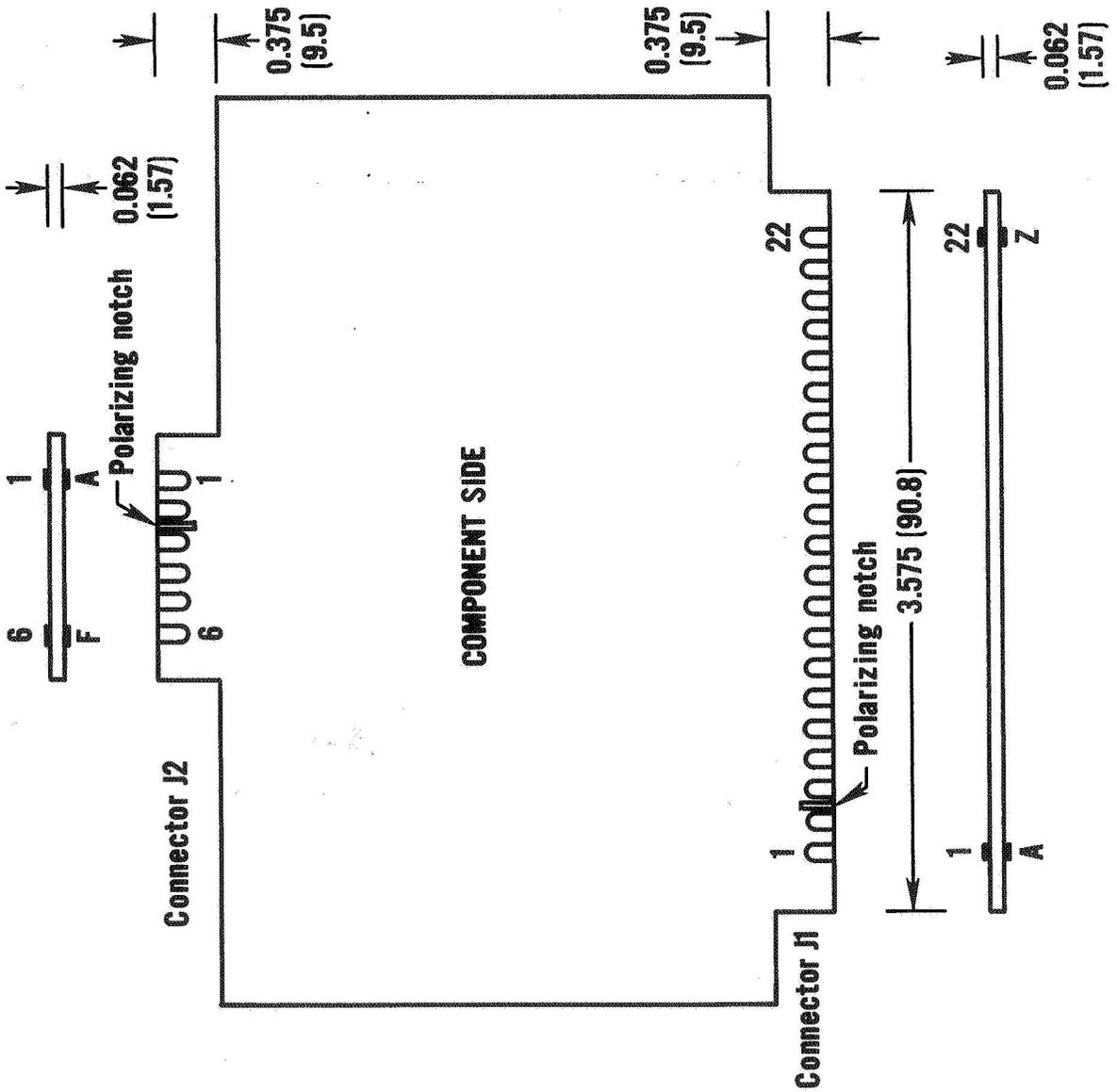


Figure A-1. Suggested printed circuit board for test data converter (dimensions in inches and (millimeters))

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET <i>(See instructions)</i>	1. PUBLICATION OR REPORT NO. NBS TN 1145	2. Performing Organ. Report No.	3. Publication Date July 1981
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5. AUTHOR(S) T.M. Souders, D.R. Flach, and B.A. Bell			
6. PERFORMING ORGANIZATION <i>(If joint or other than NBS, see instructions)</i> NATIONAL BUREAU OF STANDARDS DEPARTMENT OF COMMERCE WASHINGTON, D.C. 20234			7. Contract/Grant No. 8. Type of Report & Period Covered Final
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10. SUPPLEMENTARY NOTES <input type="checkbox"/> Document describes a computer program; SF-185, FIPS Software Summary, is attached.			
11. ABSTRACT <i>(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)</i> An NBS calibration service for high performance 12- to 18-bit analog-to-digital converters (ADC's) and digital-to-analog converters (DAC's) is described. The service offers comprehensive measurements of linearity, differential linearity, gain, offset, and rms input noise (for ADC's), with systematic uncertainties as low as 3 ppm. Measurements are made at a minimum of 1024 different codewords. The measurement approach, design features, test programs and data reduction techniques are documented, as are the methods of error estimation and quality control. Representative reports of tests are included for both DAC's and ADC's.			
12. KEY WORDS <i>(Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)</i> analog-to-digital converter; calibration service; data converter; differential linearity; digital-to-analog converter; error measurement; gain; input noise; linearity; offset.			
13. AVAILABILITY <input checked="" type="checkbox"/> Unlimited <input type="checkbox"/> For Official Distribution. Do Not Release to NTIS <input checked="" type="checkbox"/> Order From Superintendent of Documents, U.S. Government Printing Office, Washington, D C 20402. <input type="checkbox"/> Order From National Technical Information Service (NTIS), Springfield, VA 22161			14. NO. OF PRINTED PAGES 73 15. Price